

# Compal Confidential

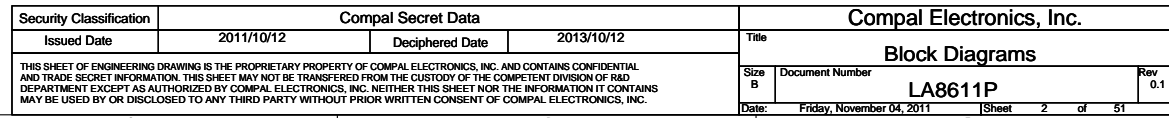
## QAWGH Schematics Document

AMD APU Trinity FS1r2 + FCH Hudson-M3 + GPU Seymourr XT

2011-10-07

REV:0.1

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+1.0VGS	1.0V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	EMC1403(VGA, DDR,WLAN)	1001-101xb	9AH
			SB-TSI (default)	1001-100xb	98H
			VGA Thermal	1000-001xb	82H
			Cap Sensor	1000-0000b	80H
			RTDS2132S-E	1010-1000b	A8H

SM Bus Controller 0

(FCH\_SMB1 ~ FCH\_SMB4, SMB\_ALERT#)

Device	Address	HEX
--------	---------	-----

SM Bus Controller 1

(FCH\_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90H
DDR DIMM2 (FCH_SMB0)	1001-001xb	92H
WLAN (FCH_SMB0)		

FCH Hudson-M2/3 SATA Port List

SATA0	NC
SATA1	HDD
SATA2	ODD
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List

APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Right USB1
Port1	Right USB2
Port2	Mini PCIE
Port3	USB Camera
Port4	BT
Port5	Card Reader
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	USB3.0 LP1
Port11	USB3.0 LP2
Port12	NC
Port13	NC

FCH Hudson-M2/3 USB OC PIN

USB_OC0#	USB3.0 (LP1, LP2)
USB_OC1#	USB2.0 (RP1)
USB_OC2#	USB2.0 (RP2)
USB_OC3#	NC
USB_OC4#	NC
USB_OC5#	NC
USB_OC6#	NC
USB_OC7#	NC

BOM Structure

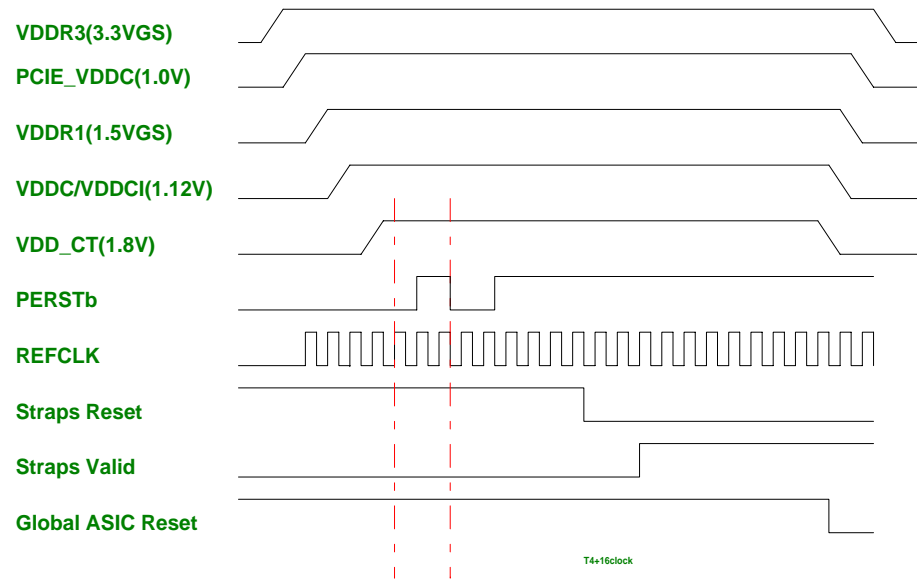
UMA@ : UMA only  
PX@ : DIS muxluss  
CMOS@ : USB camera  
HDMI@ : HDMI function  
nonHDMI@ : w/o HDMI function  
BT@ : BT function  
ME@ : ME components  
X76@ : VRAM  
45@ : 45 Level  
PX4@ : PX4  
PX5@ : PX5  
8162@ : 10/100 LAN  
GIGA@ : giga LAN  
14@ : G 14"  
15@ : G 15"  
BBH@ : Best Buy high-end  
nonBBH@ : non Best Buy high-end  
AN@ : Apple & Nokia combo  
A@ : Apple only

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Power-Up/Down Sequence

"Seymour" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa). For BACO enabled designs, VDDC must ramp up before VDD\_CT at system power up.
- For power down, reversing the ramp-up sequence is recommended



Without BACO option :

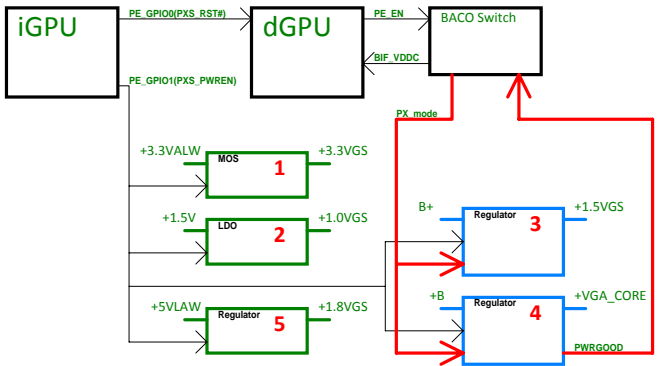
PE\_GPIO0 (PXS\_RST#) : Low -> Reset dGPU ; High -> Normal operation  
PE\_GPIO1 (PXS\_PWREN) : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

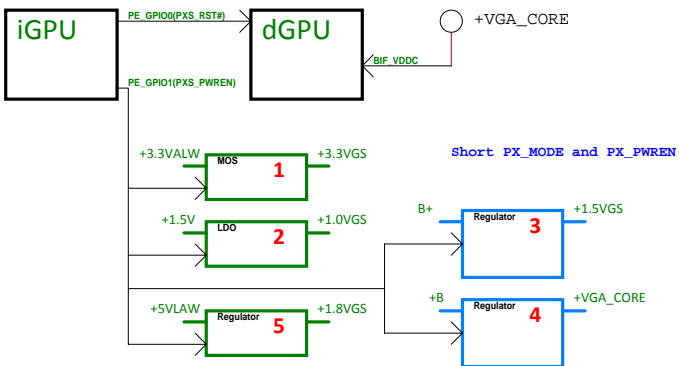
PE\_GPIO0 (PXS\_RST#) : High -> Normal operation (dGPU is not reset on BACO mode)  
PE\_GPIO1 (PXS\_PWREN) : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1D1, A2VDDQ, VDD2D1, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28

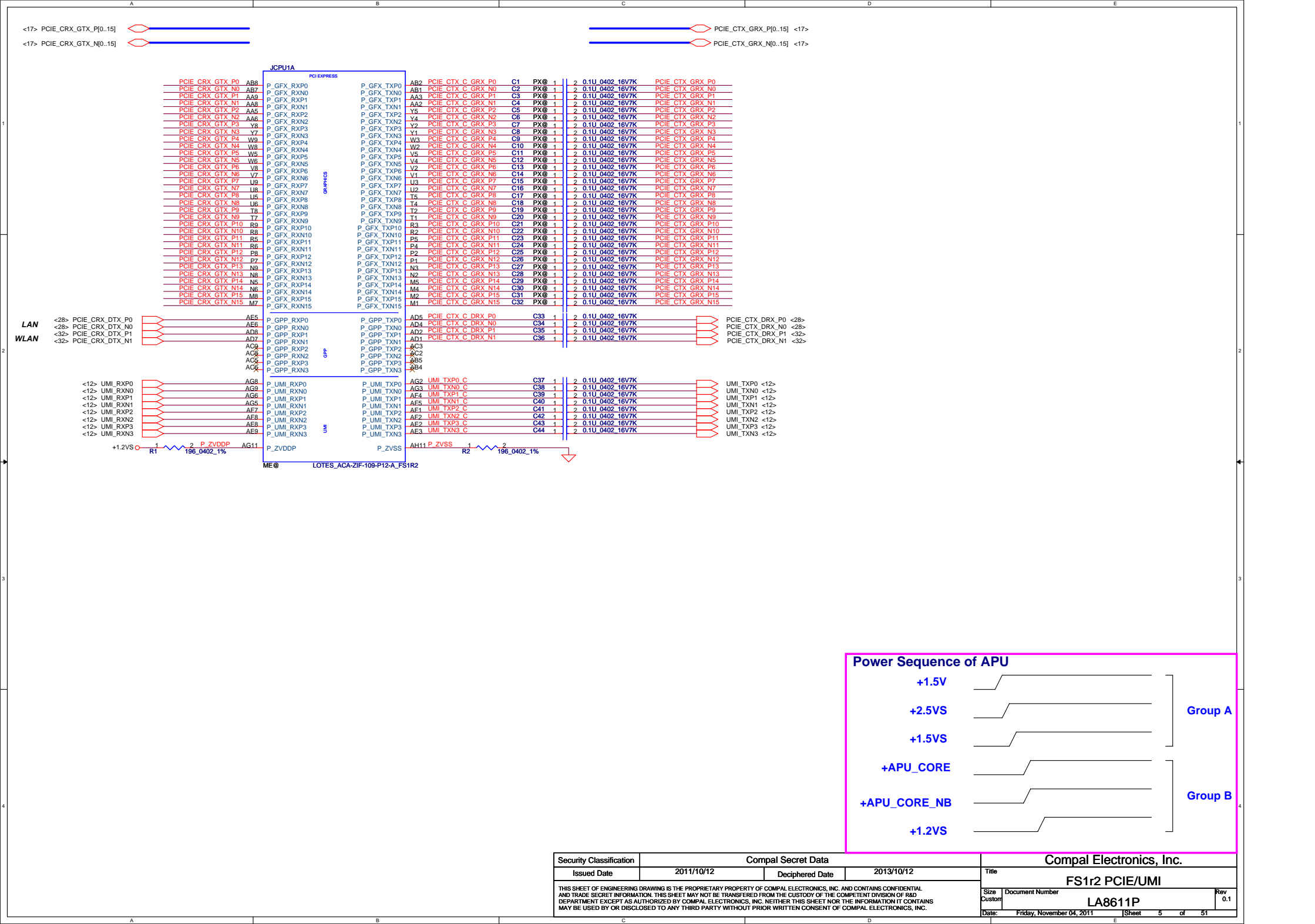
PX4.0

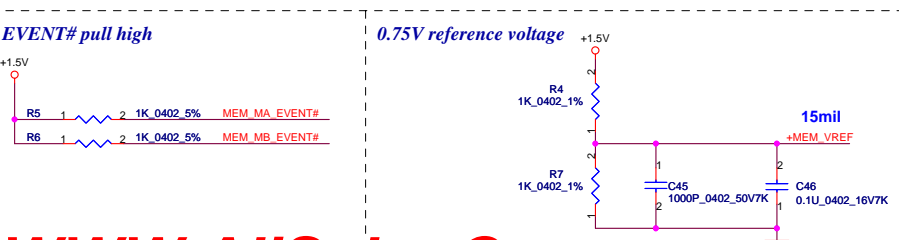
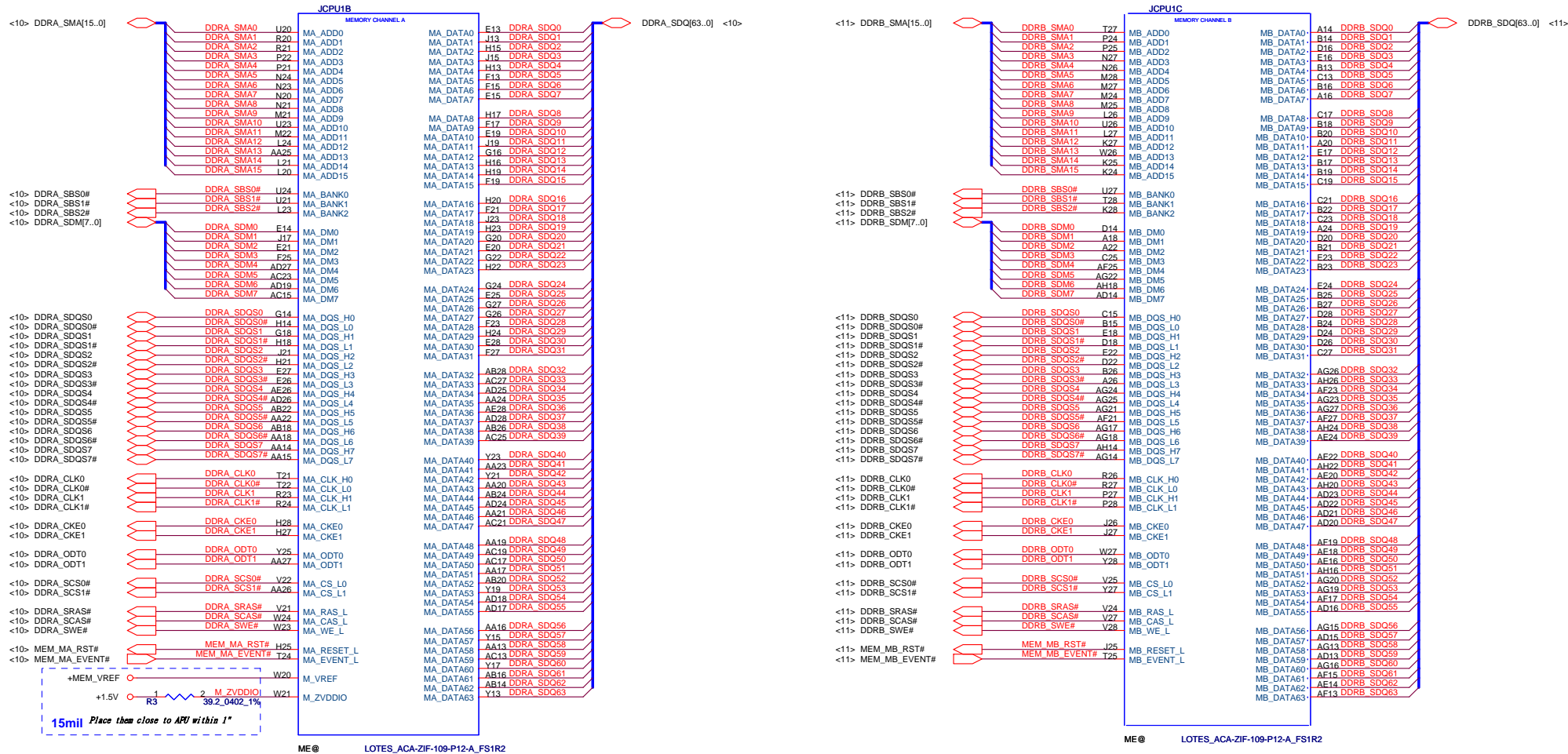


PX5.0



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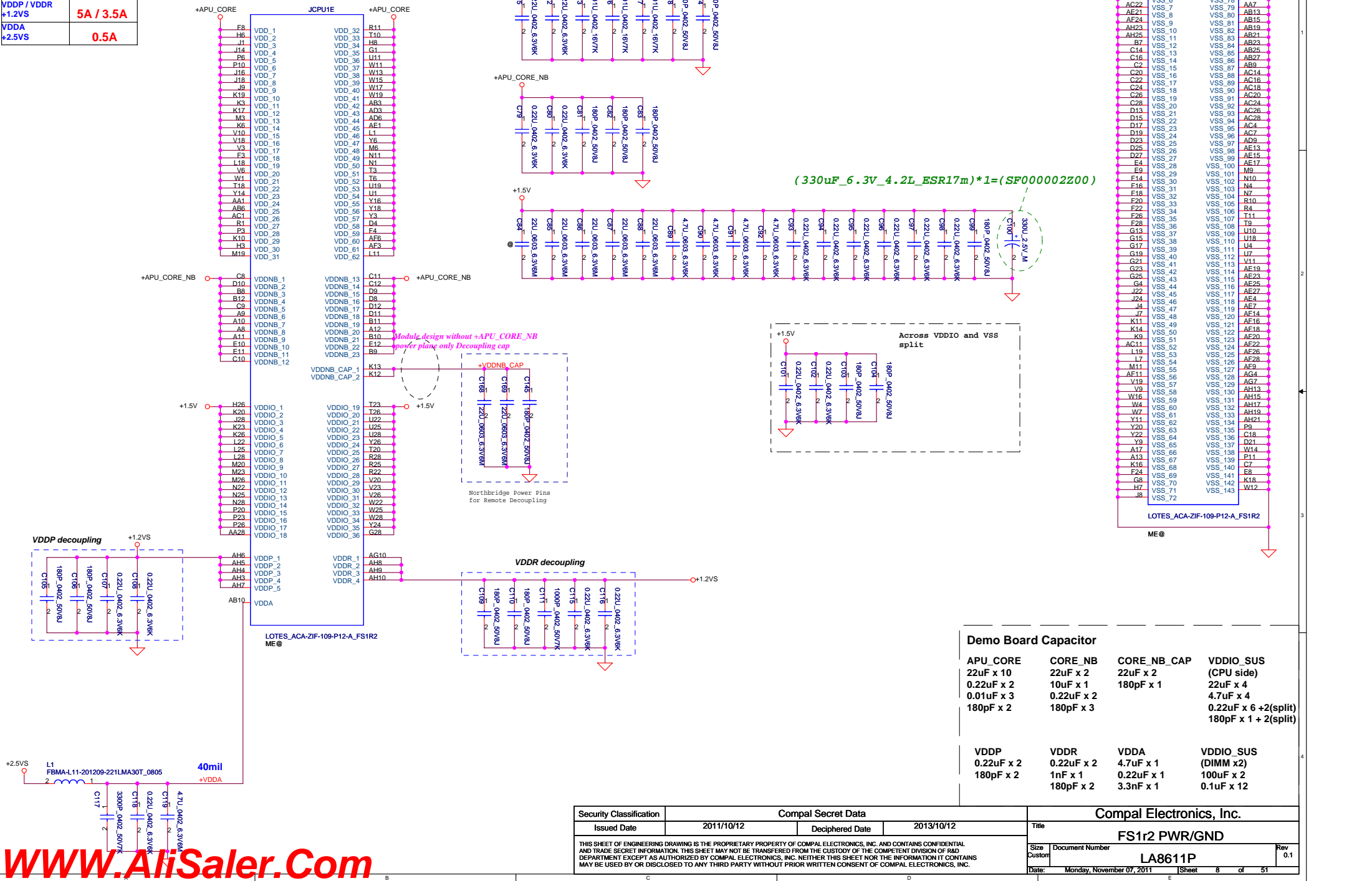
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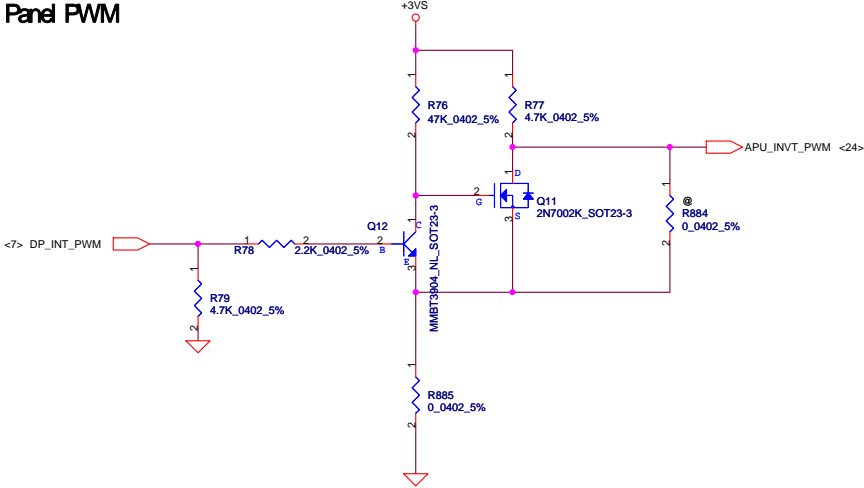
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



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						Size		Document Number		Rev	
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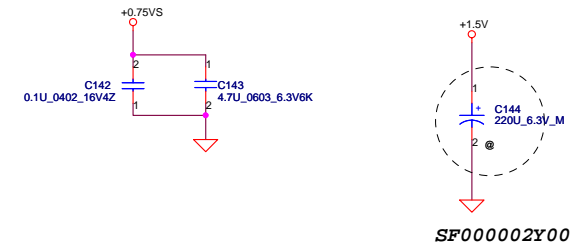
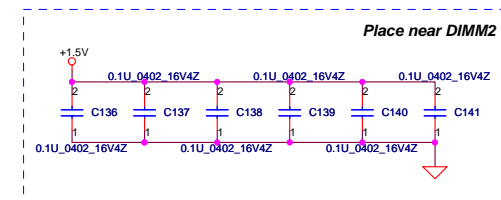
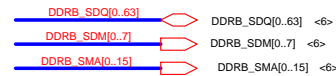


Pand PWM



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								Size	Document Number			Rev		
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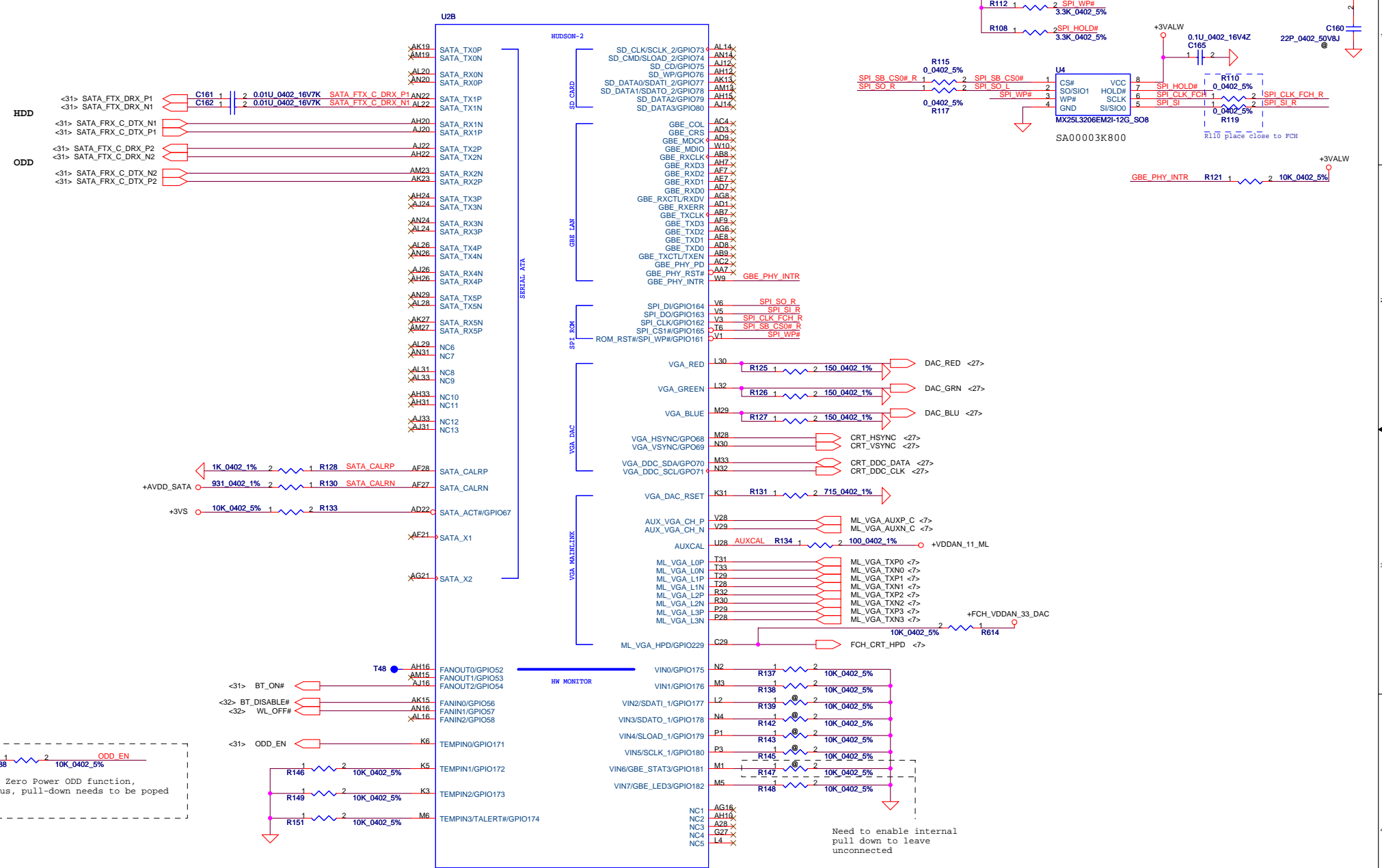


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Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title DDRIII SO-DIMM 2			
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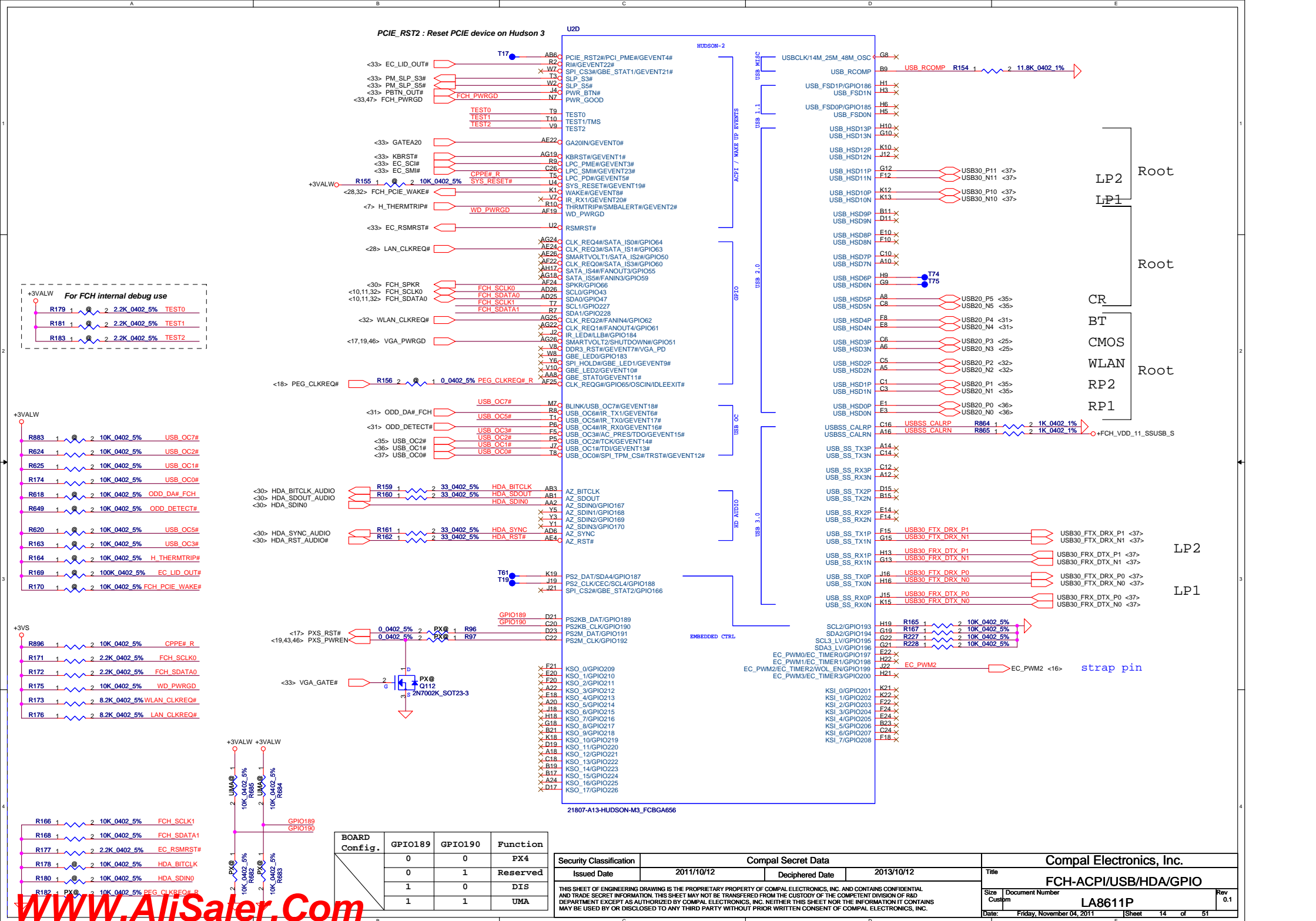


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				FCH PCIE/CLK/PC/LPC/RTC		
				Size	Document Number	Rev
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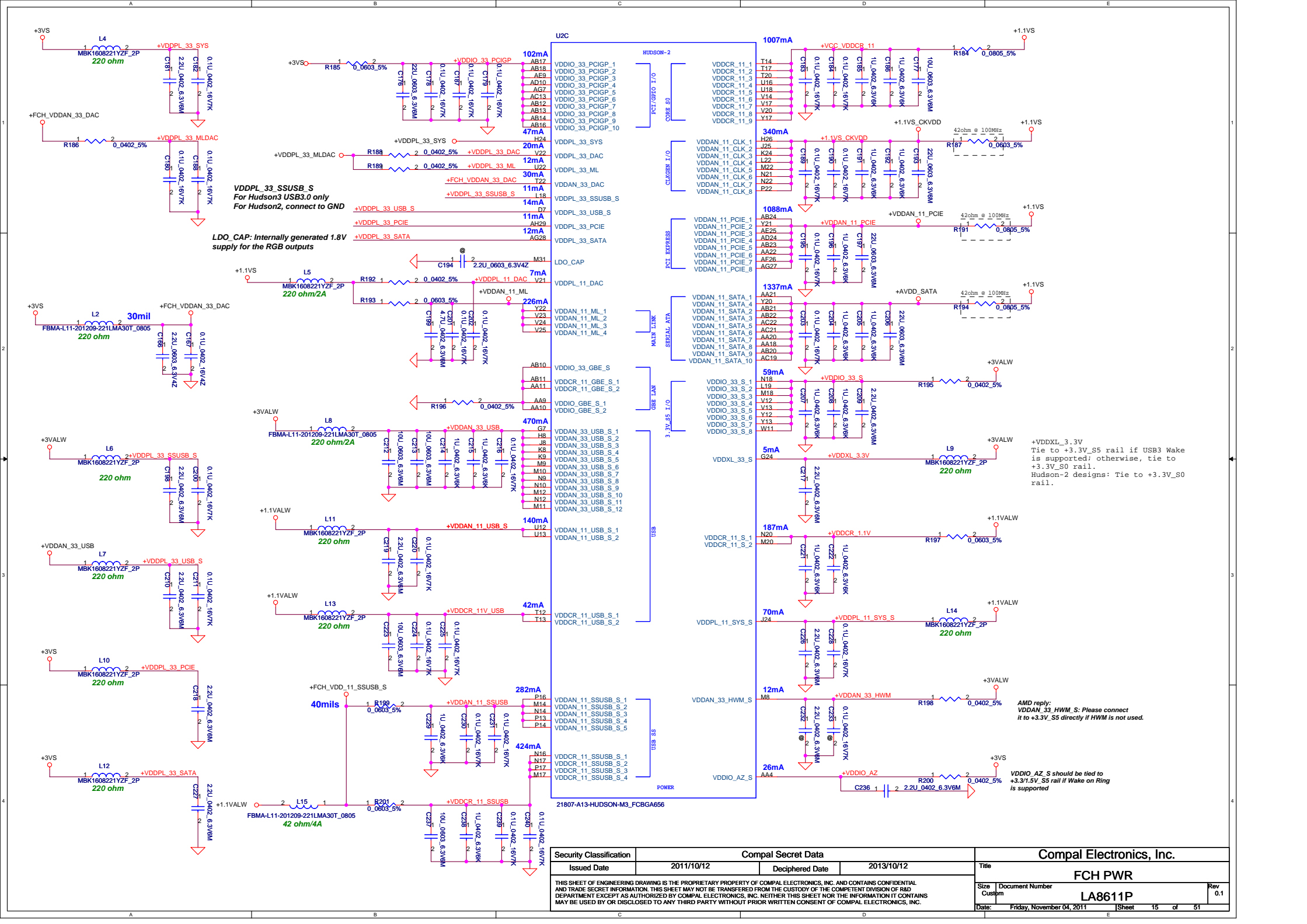
4MB SPI ROM  
& Non-share ROM.



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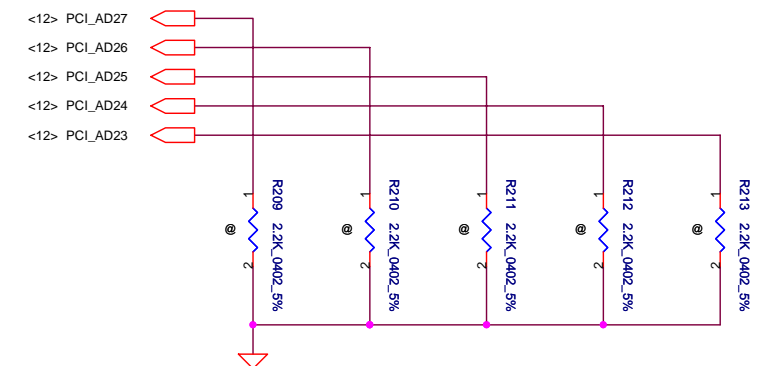
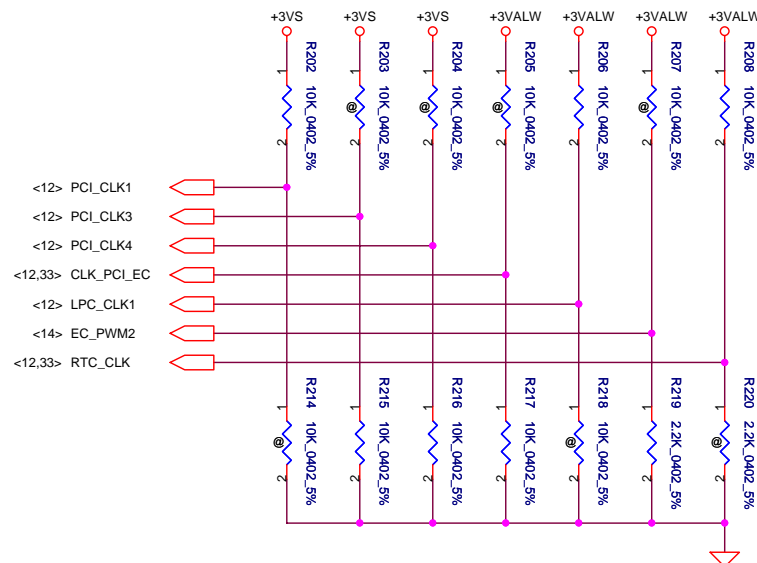
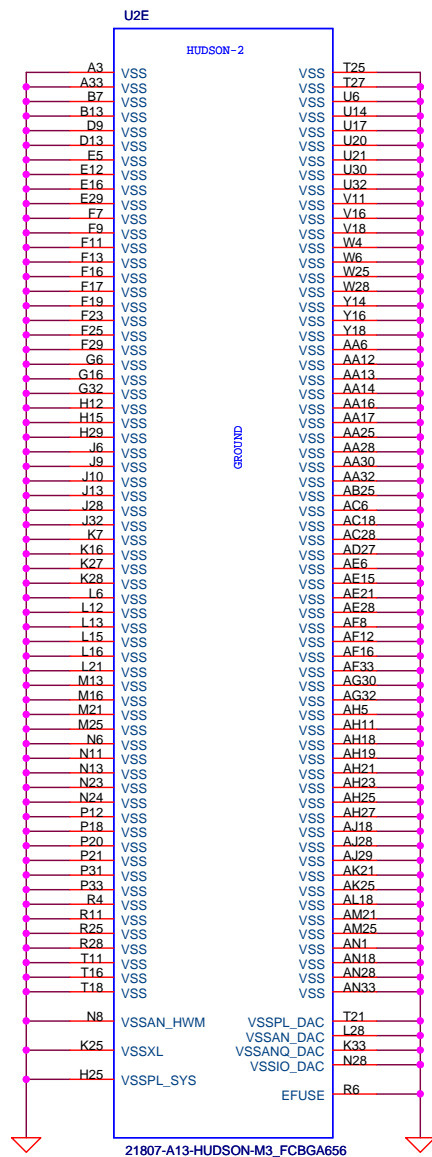




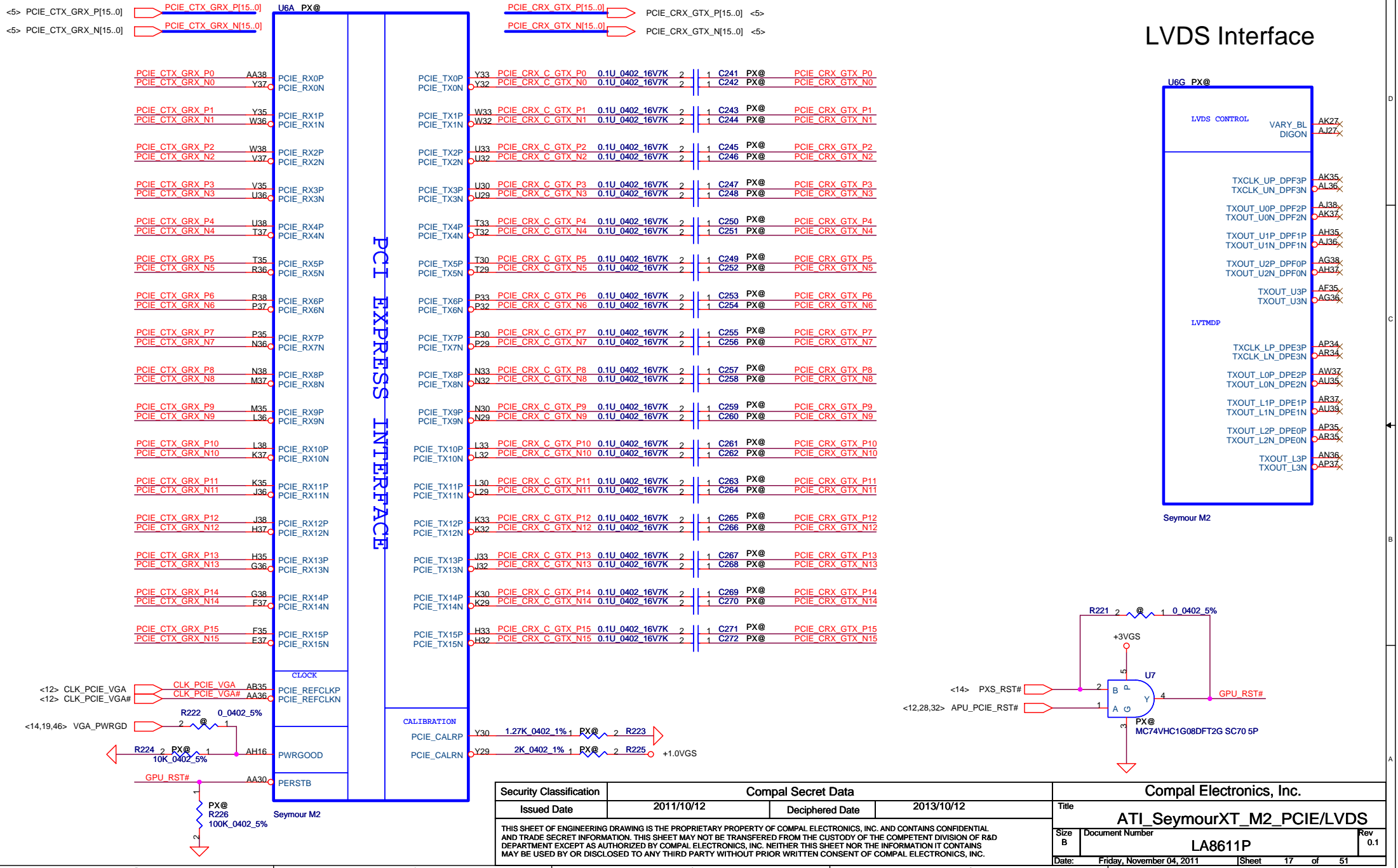
FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

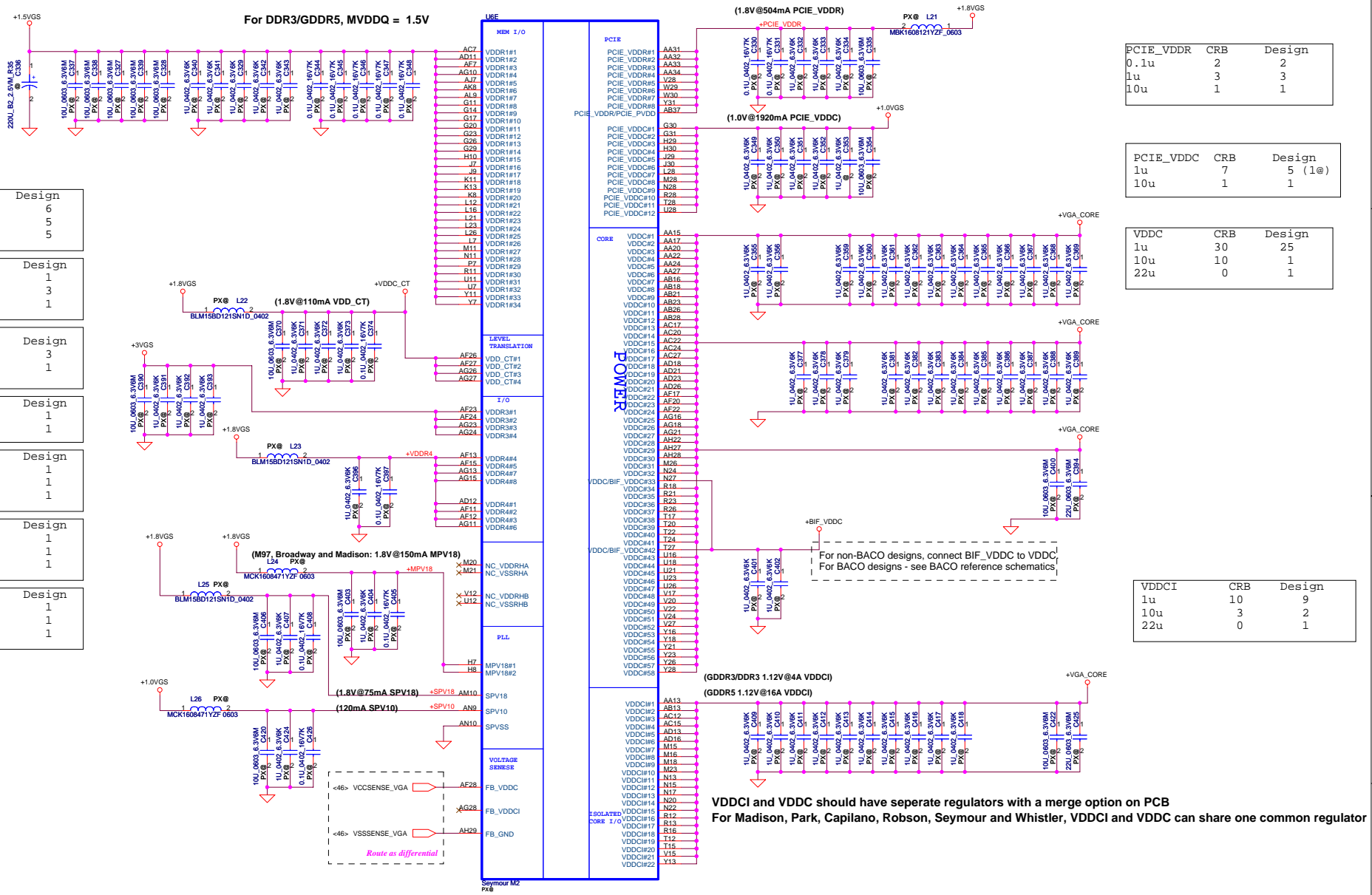
VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

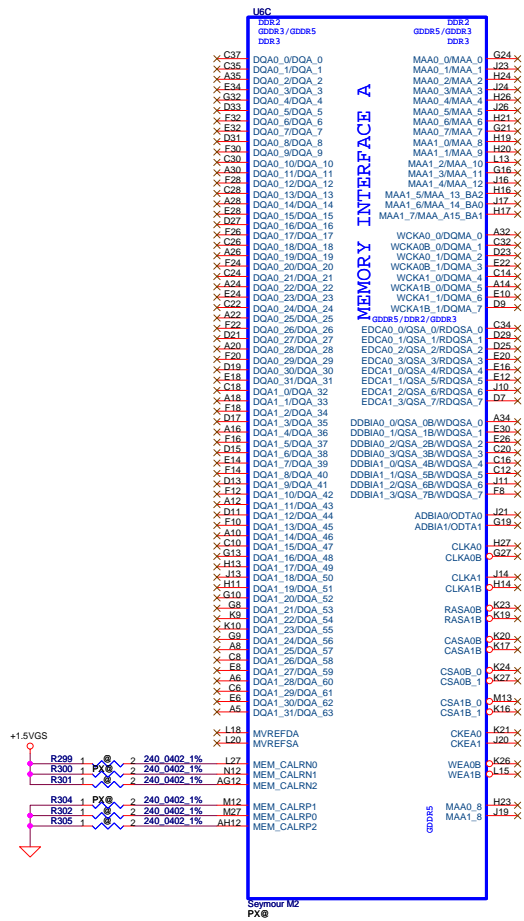
MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

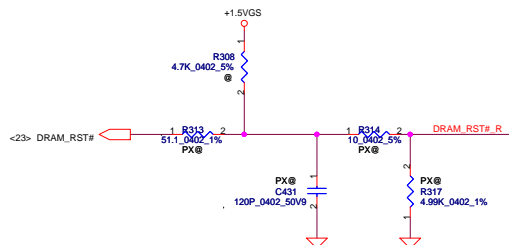
SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1



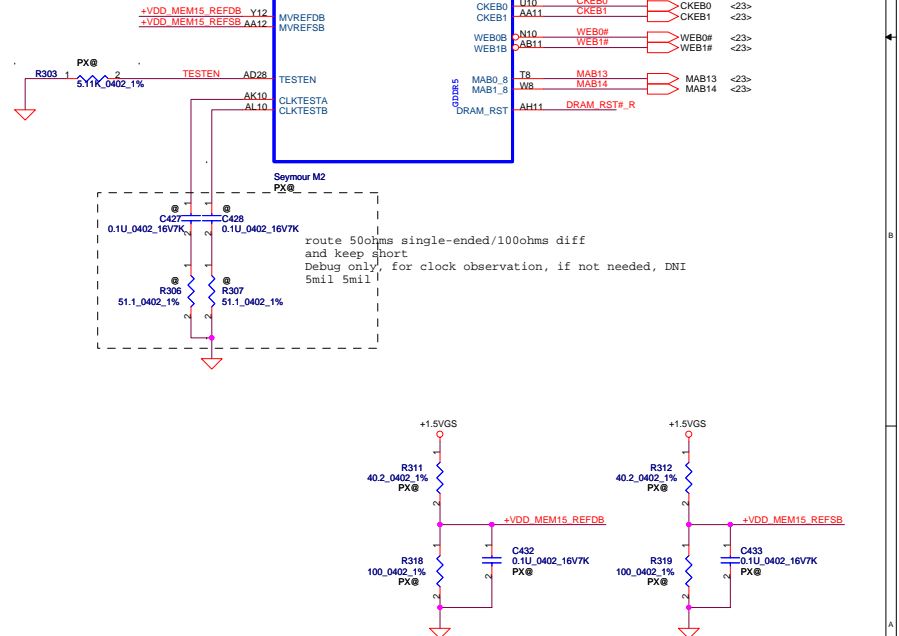




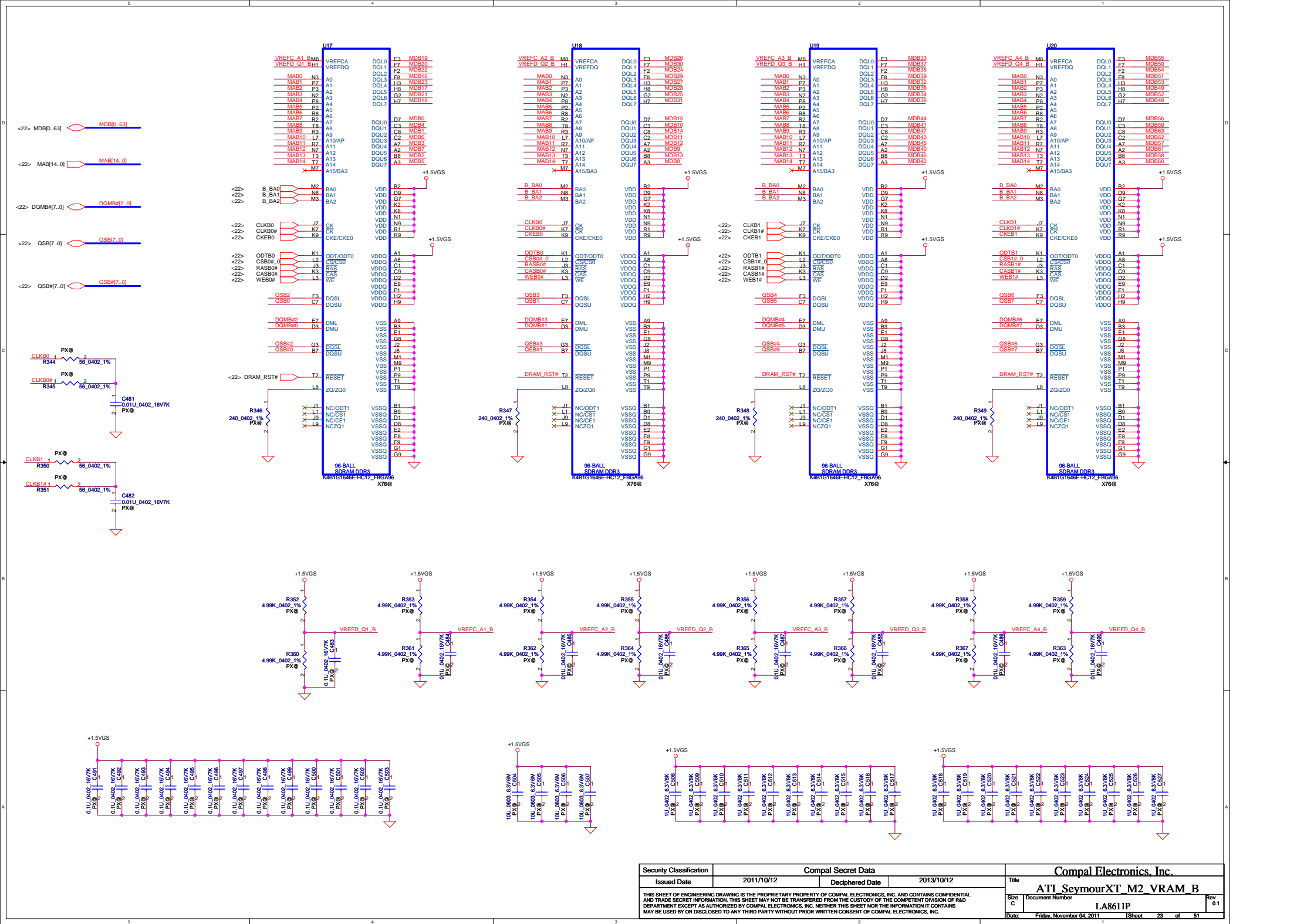
This basic topology should be used for DRAM\_RST for DDR3/DDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.  
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
ST91Q063DFR-11C	R293	R296	R298
4K1Q1646G-BC11	R294	R295	R298
ST91Q063DFR-11C	R293	R296	R297
4K1Q1646G-BC11	R294	R295	R297

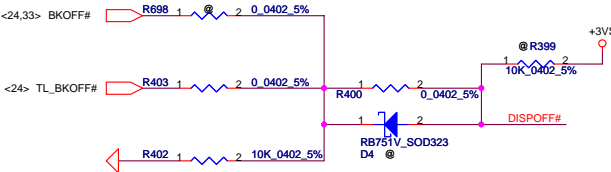
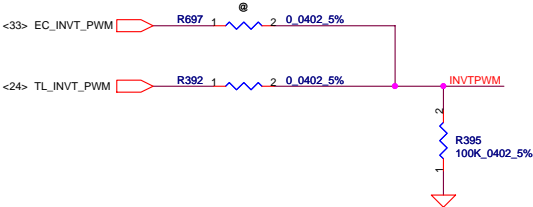
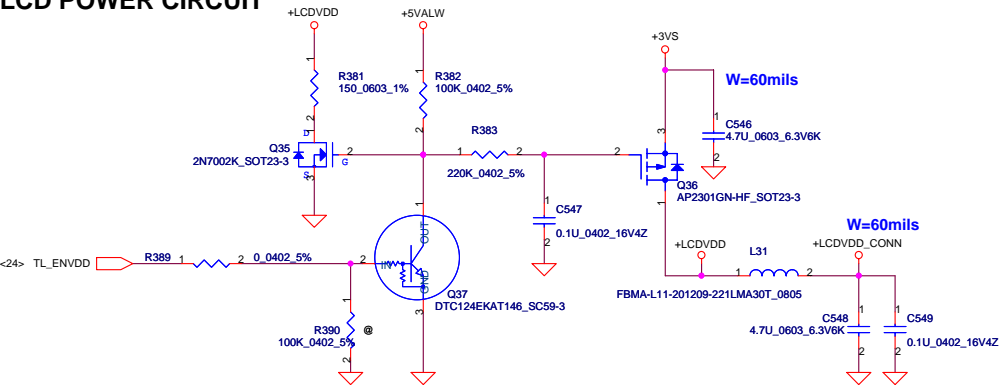




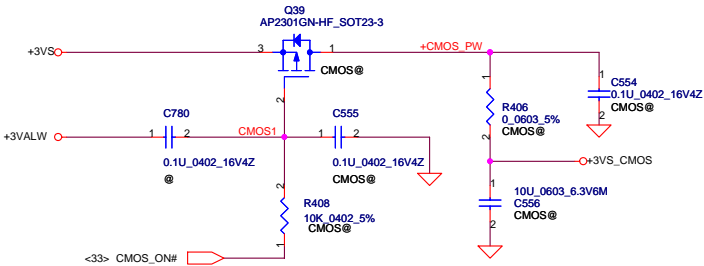




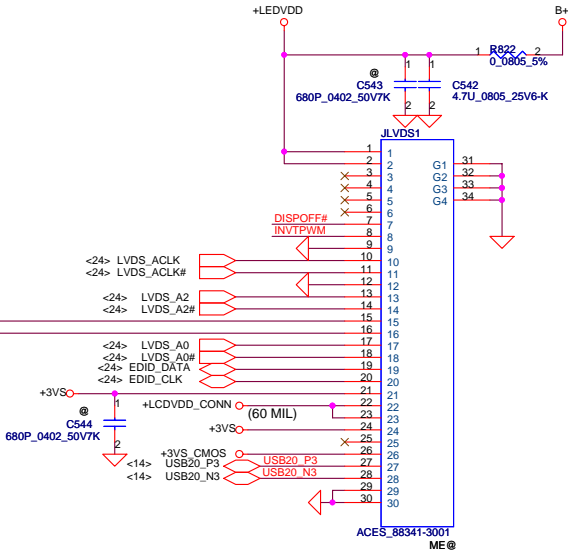
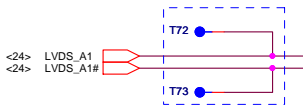
LCD POWER CIRCUIT



CMOS Camera

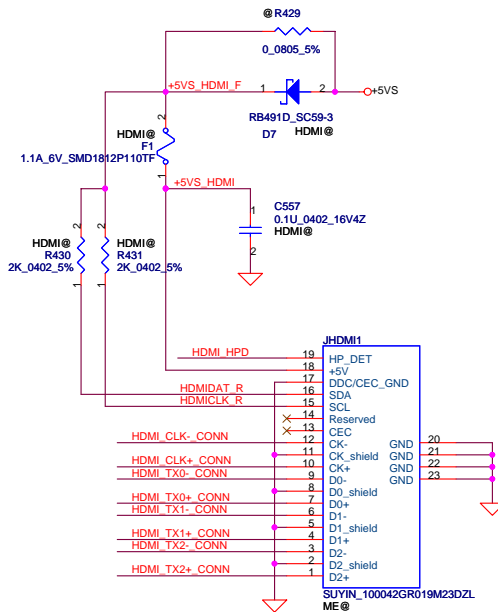
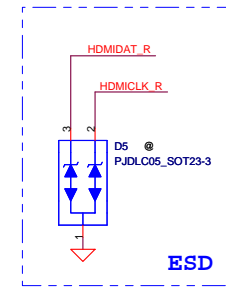
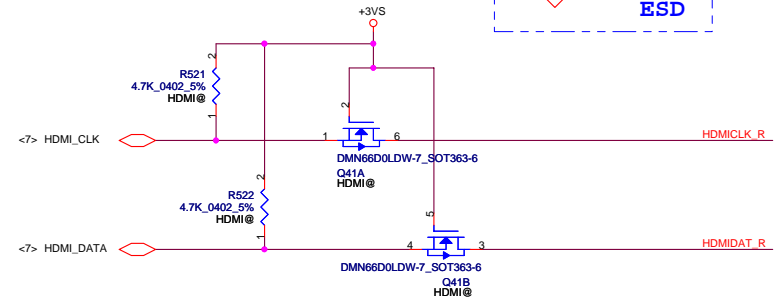
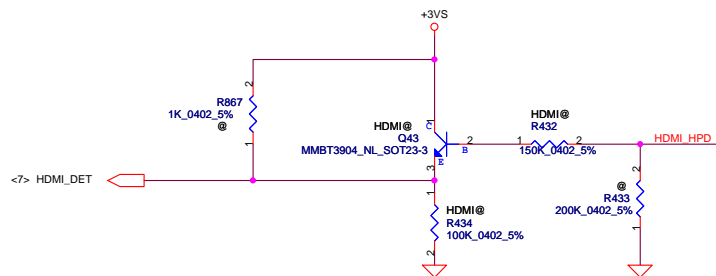
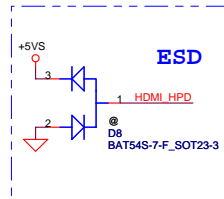
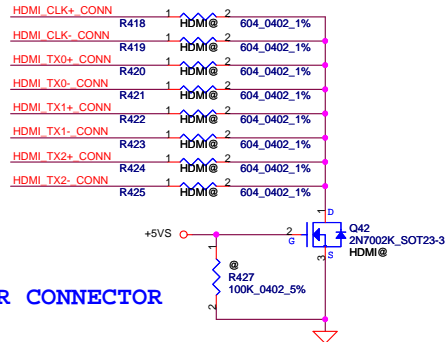
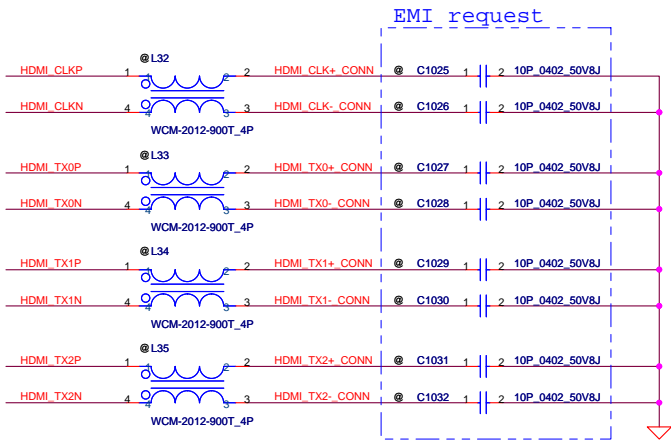


Reserve for R01 as vender request

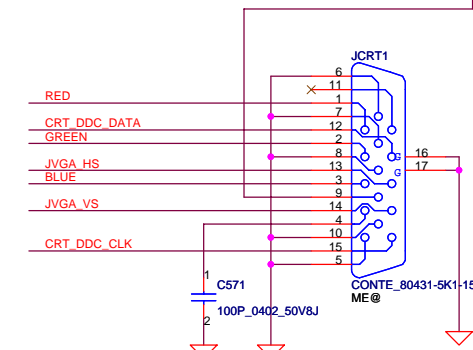
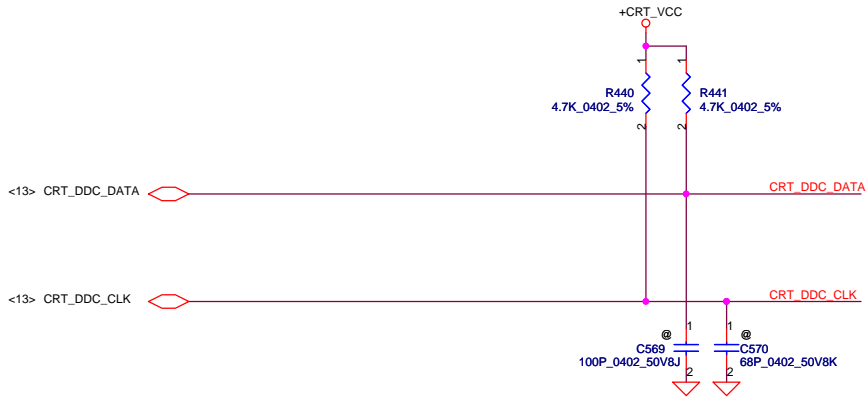
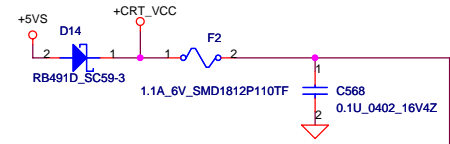
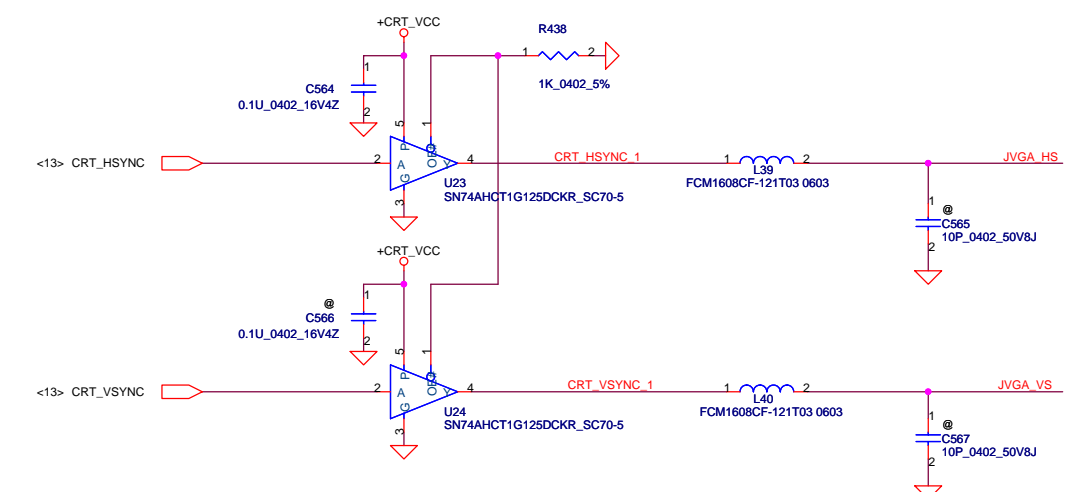
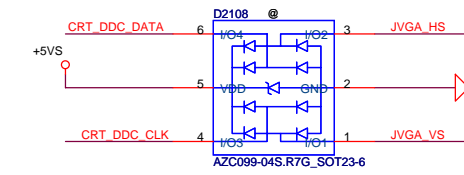
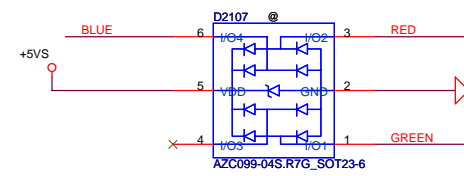
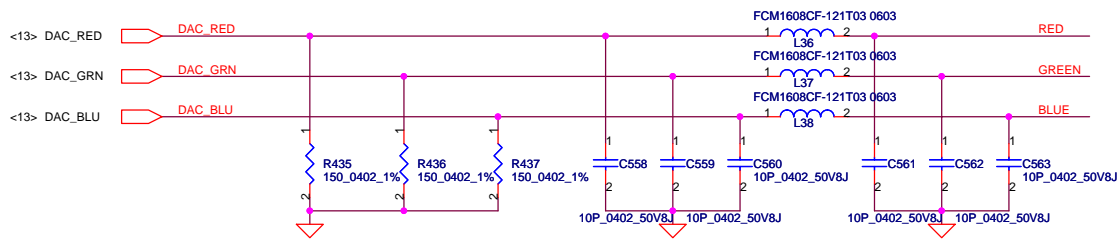


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				B	LA8611P	0.1			
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<7> HDMI_CLKP	R410	HDMI@_1	2	0.0402 5%	HDMI_CLK+_CONN
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					Size		Document Number		Rev	
					Custom		LA8611P		0.1	
					Date:		Friday, November 04, 2011		Sheet 26 of 51	

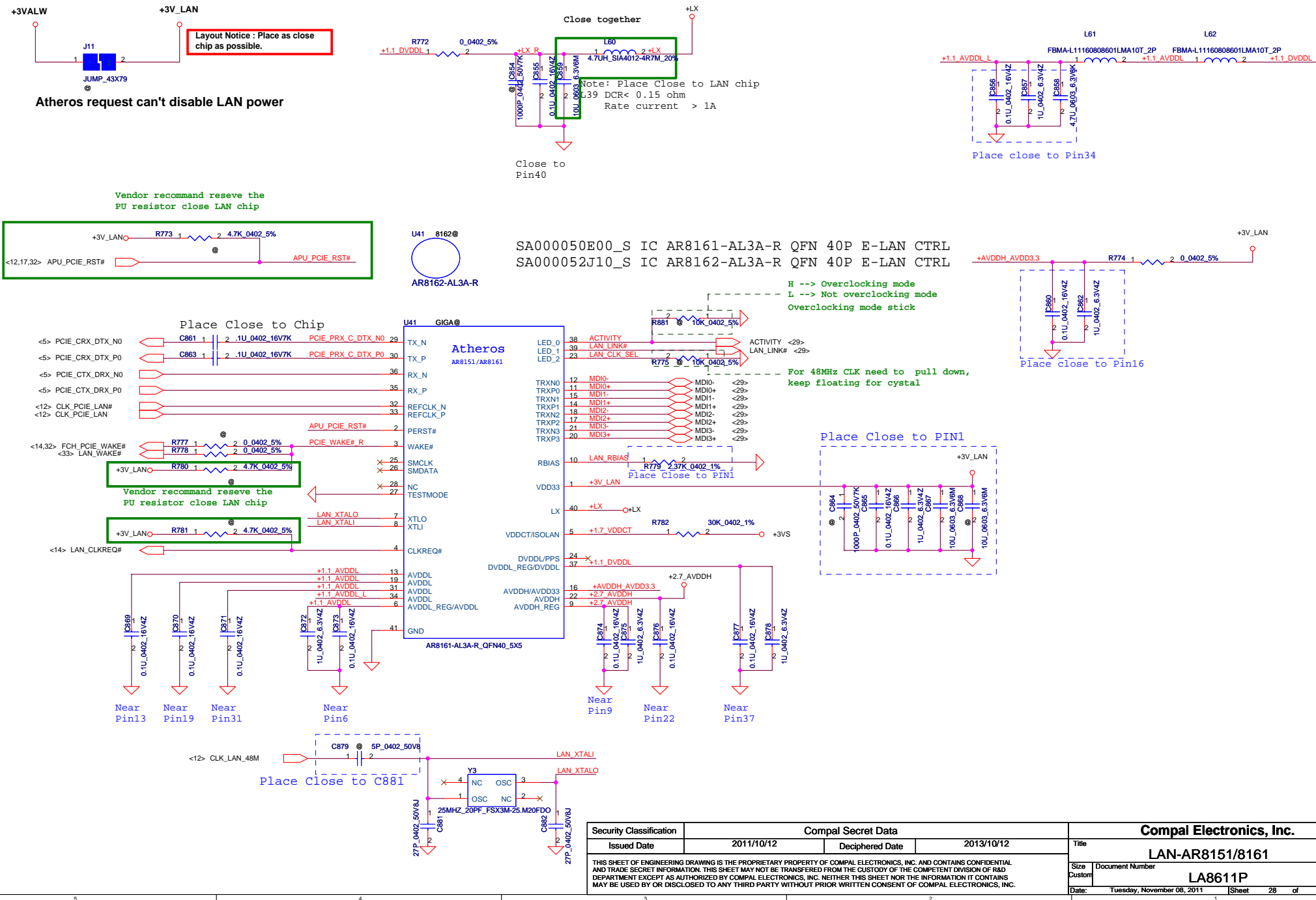


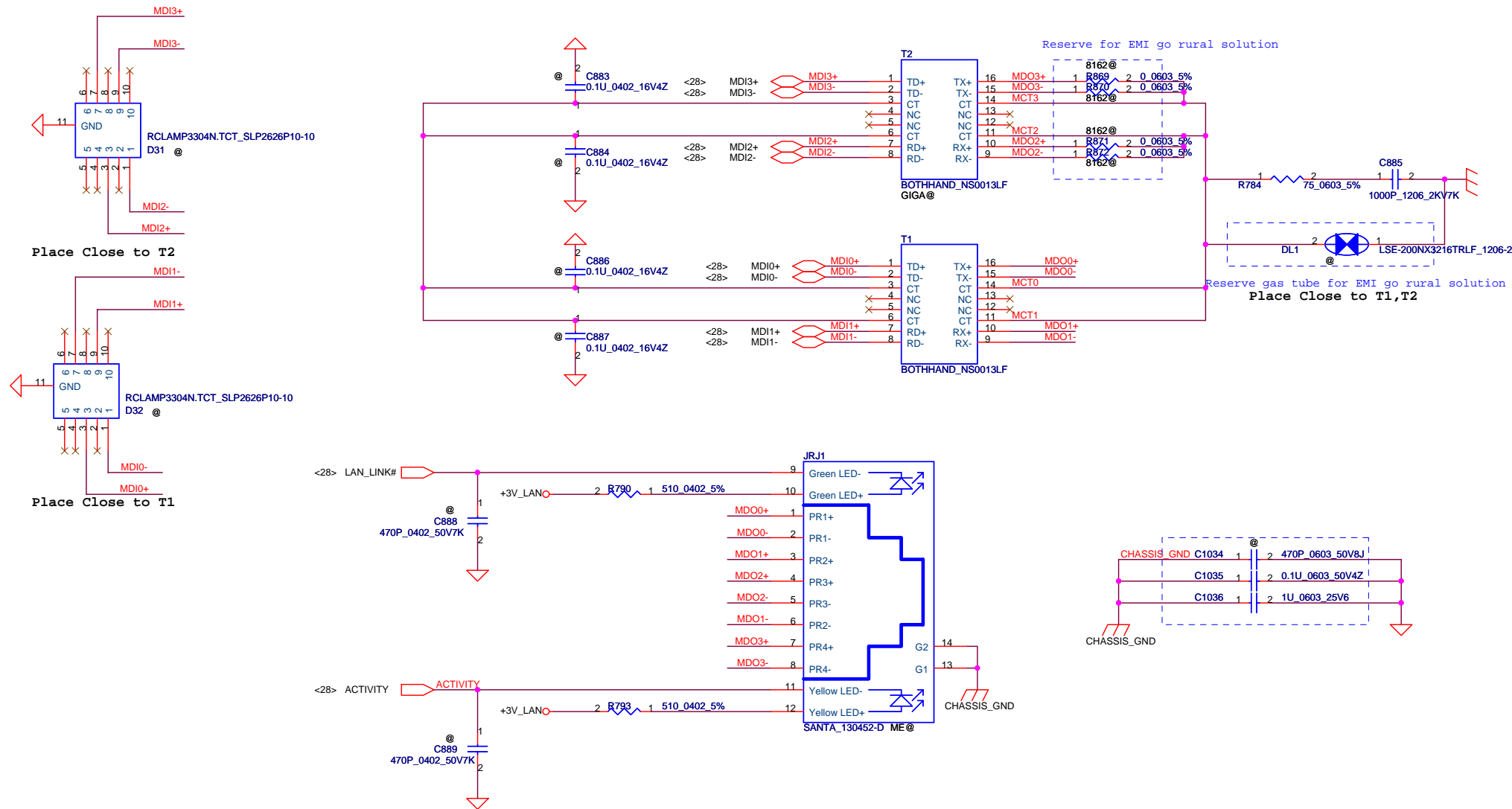
Security Classification		Compal Secret Data		Title	
Issued Date	2011/10/12	Deciphered Date	2013/10/12	CRT Connector	
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				Date: Friday, November 04, 2011	Sheet 27 of 51

**Compal Electronics, Inc.**

**LA8611P**

# Switching Mode only



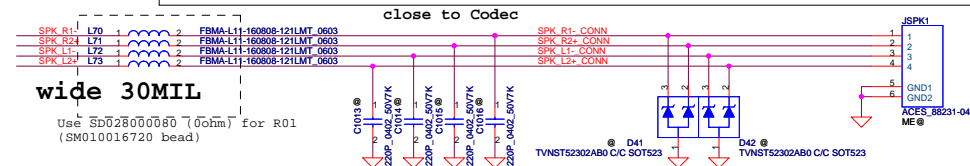
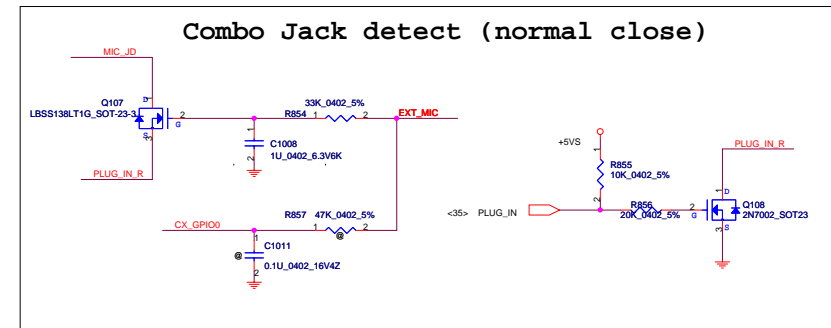
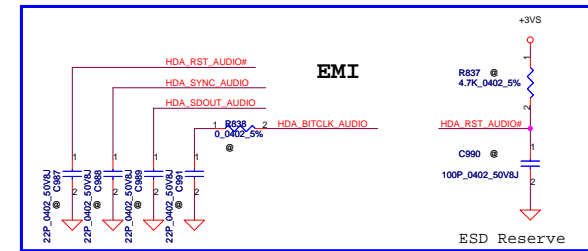
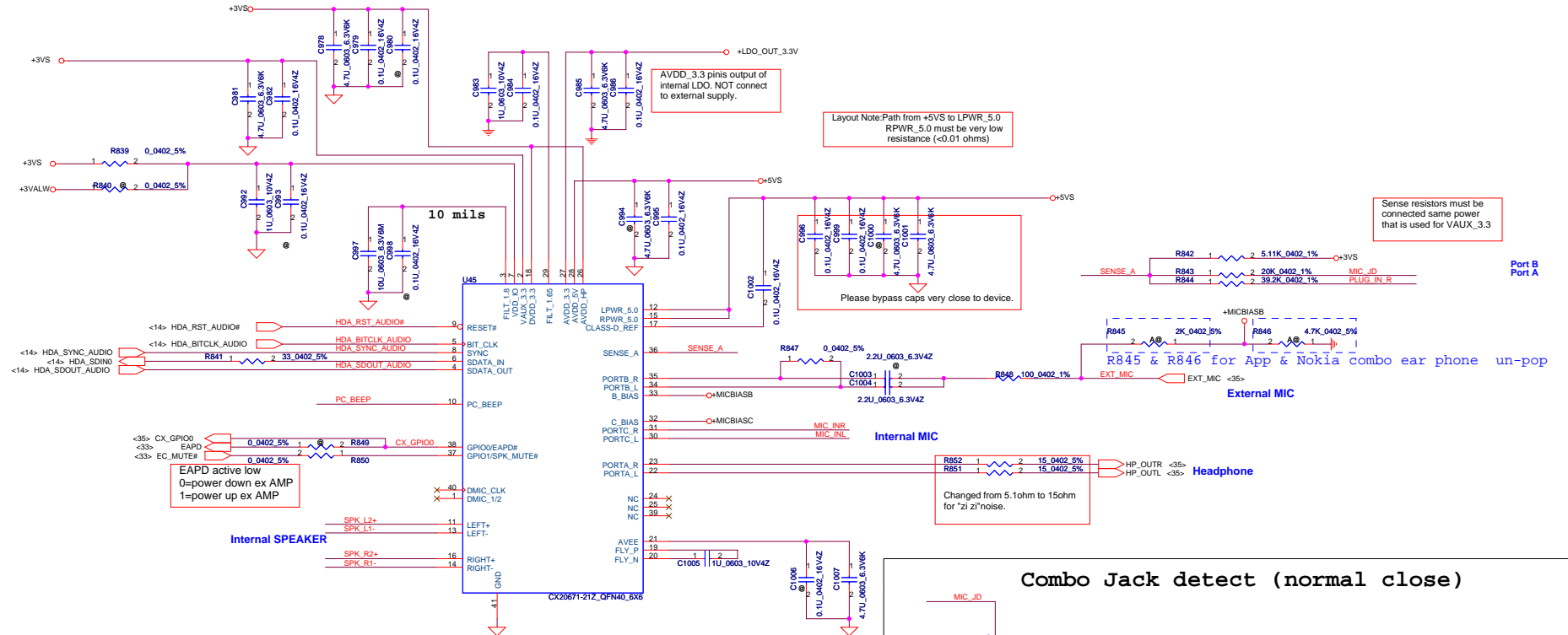


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/10/12		Deciphered Date		2013/10/12		Title	
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										Size	
										Document Number	
										LA8611P	
										Date: Tuesday, November 08, 2011	
										Sheet 29 of 51	
										Rev 0.1	

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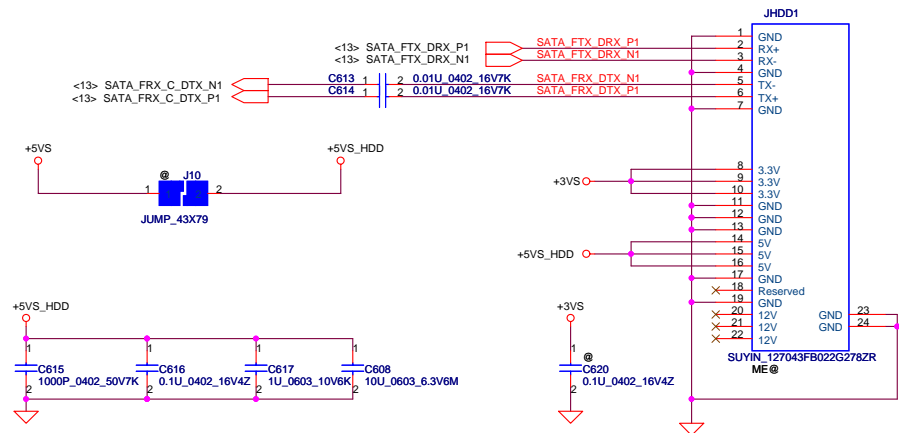


CX20671  
High Definition Audio Codec SoC  
With Integrated Class-D Stereo  
Amplifier.  
An integrated 5 V to 3.3 V Low-dropout  
voltage regulator (LDO).  
An integrated 3.3 V to 1.8V Low-dropout  
voltage regulator (LDO).

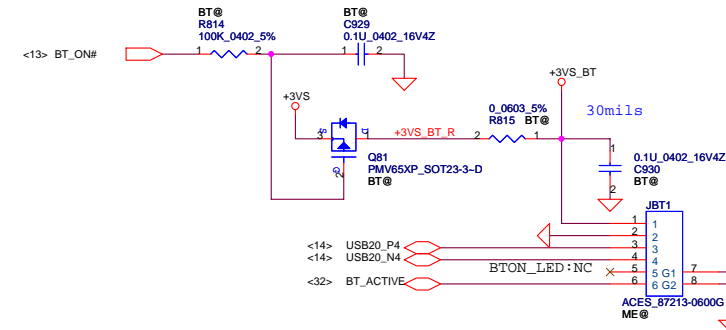


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				LA8611P	Rev 0.1
				Date: Monday, November 07, 2011	Sheet 30 of 51

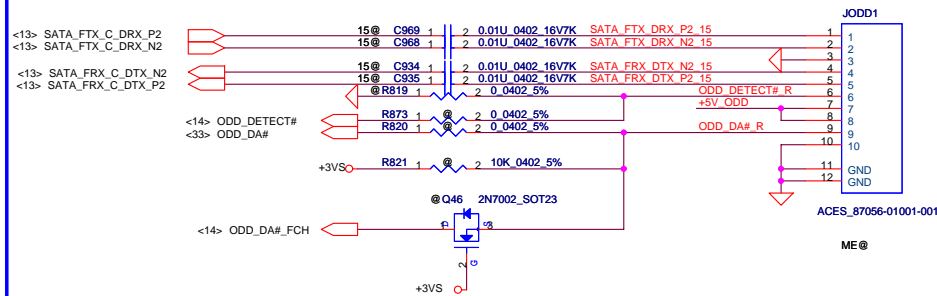
## HDD CONN



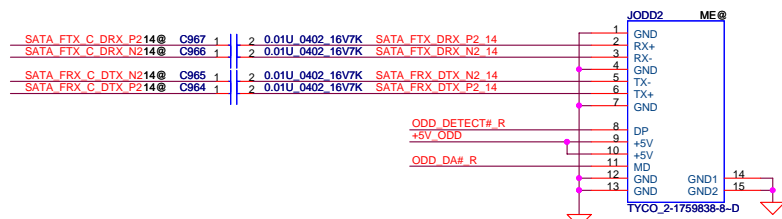
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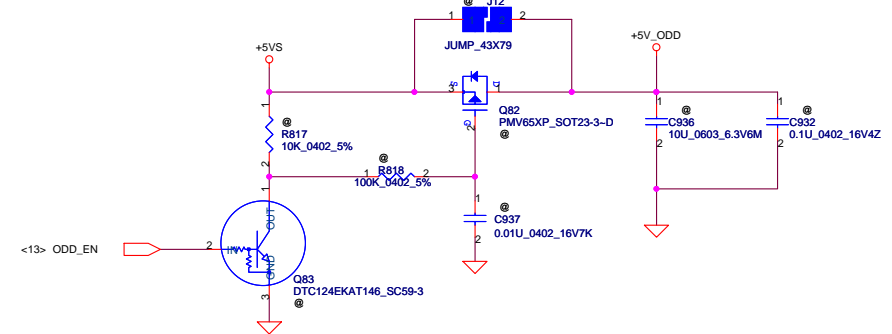
## ODD CONN 15"



## ODD CONN 14"

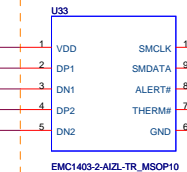
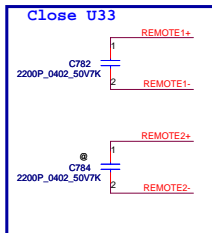


short J12, no zero power ODD function

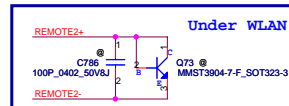


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Issued Date				2011/10/12				Title			
Deciphered Date				2013/10/12				HDD/ODD/BT			
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Date: Friday, November 04, 2011				Document Number				LA8611P			
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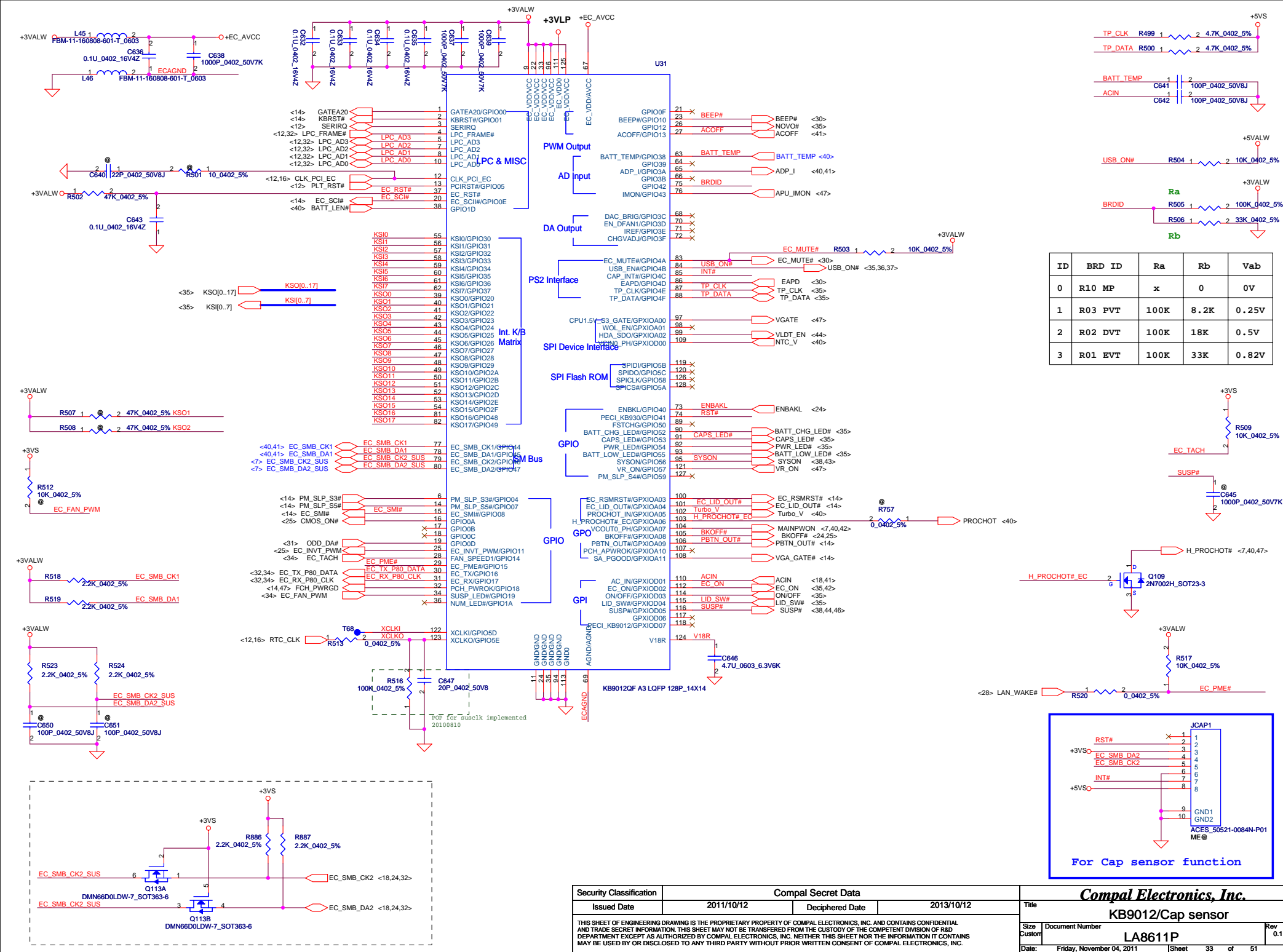
**WWW.AliSaler.Com**



Change from SA000029210 to SA000046C00 for main source



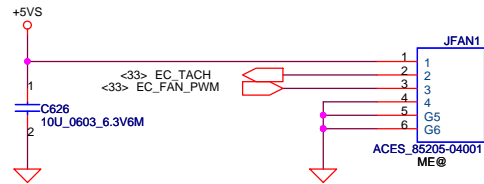
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>			
Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title	Mini PCIE/Thermal IC		
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				LA8611P			0.1
				Date:	Friday, November 04, 2011	Sheet	32 of 51



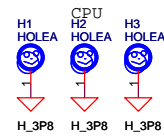
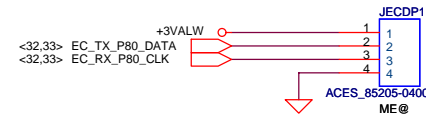
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1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

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Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title	KB9012/Cap sensor	
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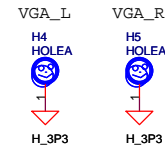
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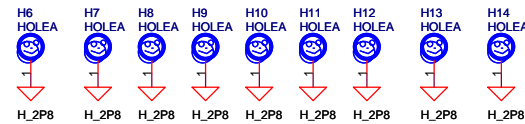
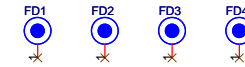
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A

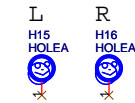


B



D

M/B 橢圓孔



H\_3P0X4P0N H\_3P0X4P0N

M/B 圓孔



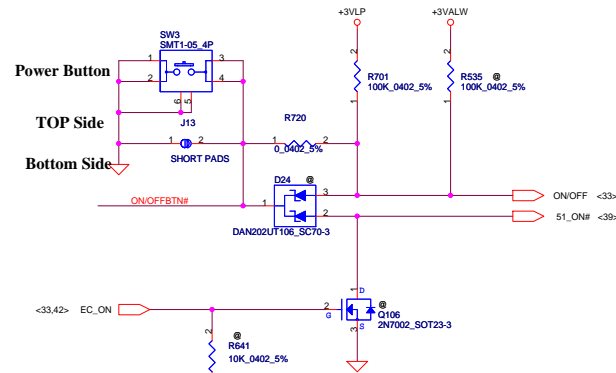
H\_3P0N

E

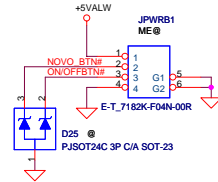
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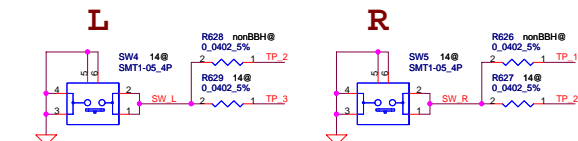
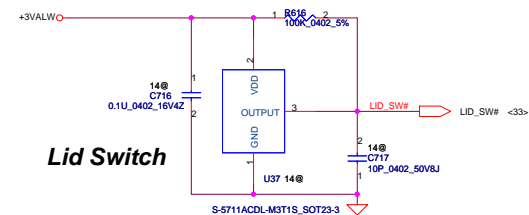
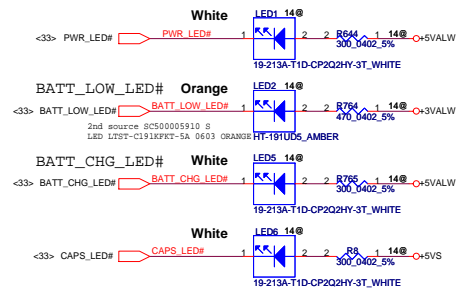
## ON/OFF switch



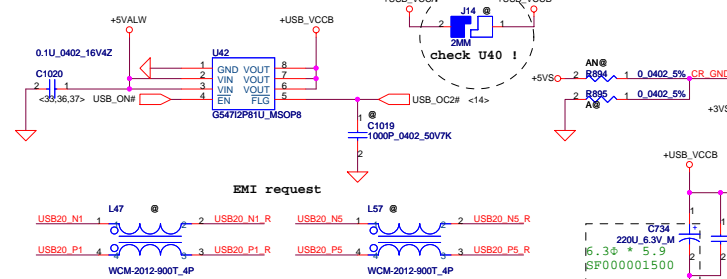
## Power Button Board Conn. 8pin



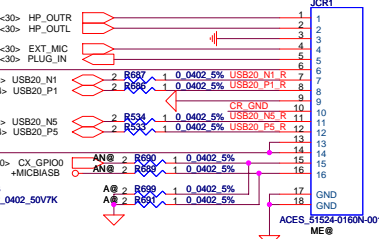
## FOR 14"



## IO board USB port

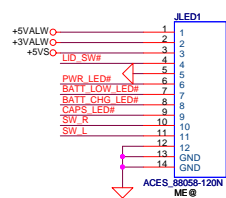


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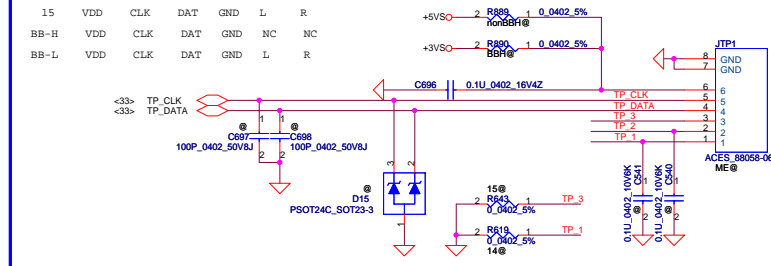


## FOR 15"

### LED B/D Conn



## To TP/B Conn.

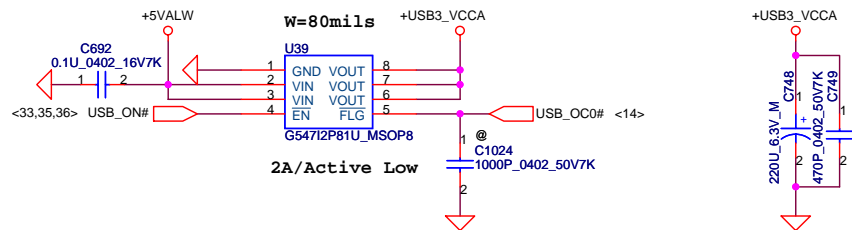


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Compal Electronics, Inc.		KBD/PWR/CR/LED/TP Conn.	
LA8611P		Rev 0.1	

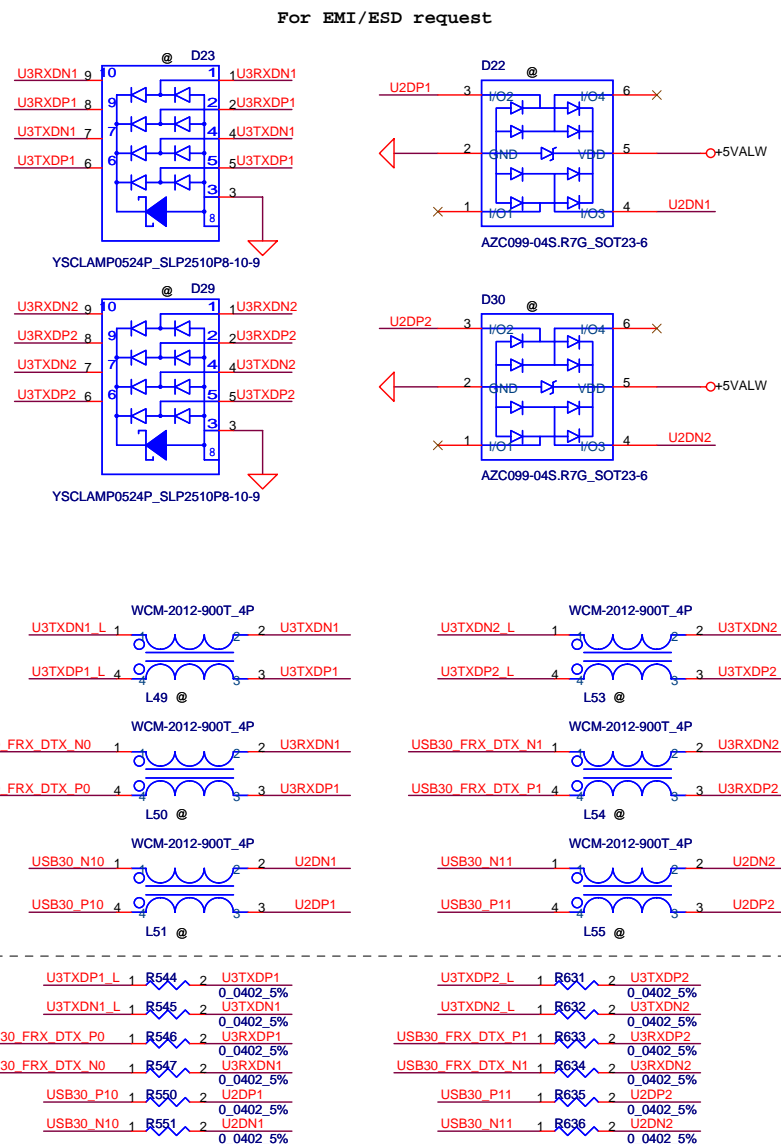
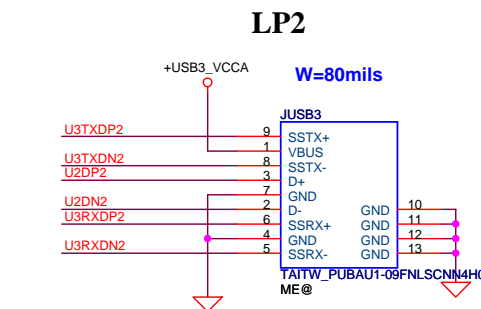
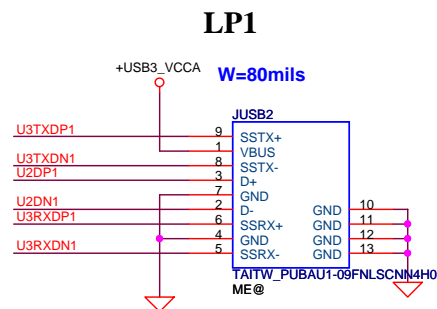
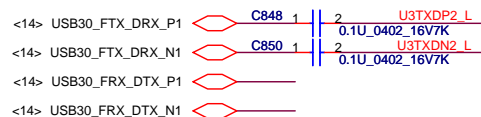
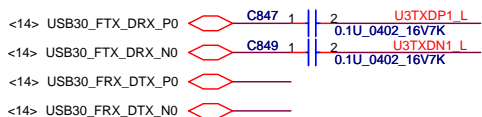






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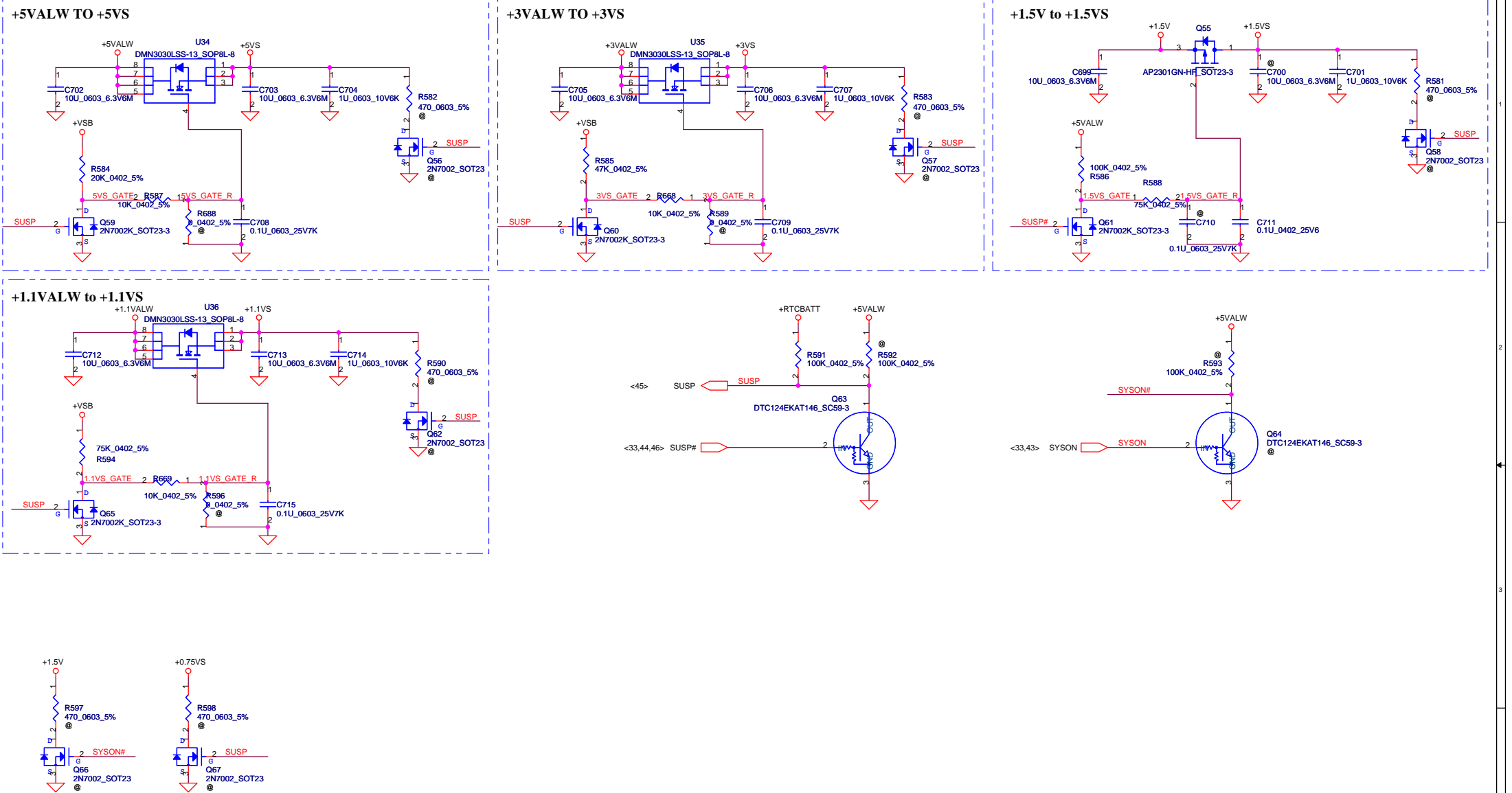


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				Document Number	0.1
				Date:	Friday, November 04, 2011
				Sheet	37 of 51

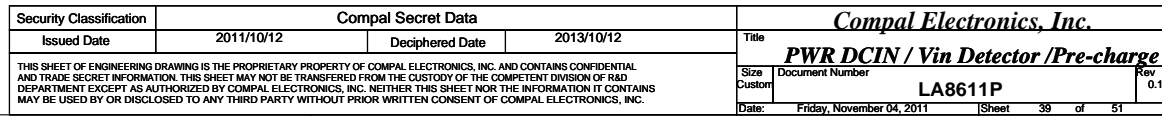
**Compal Electronics, Inc.**

Left USB3.0

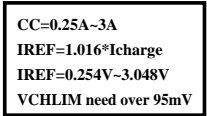
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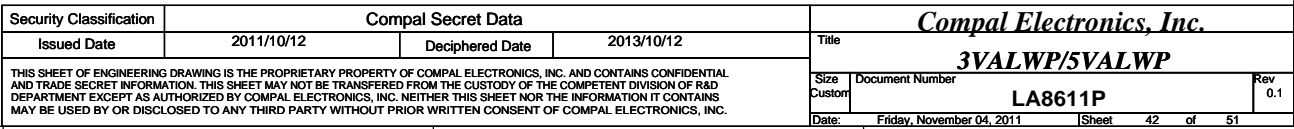
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title		
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				Size	Document Number	Rev
				Cuspm	LA8611P	0.1
				Date:	Tuesday, November 08, 2011	Sheet 38 of 51

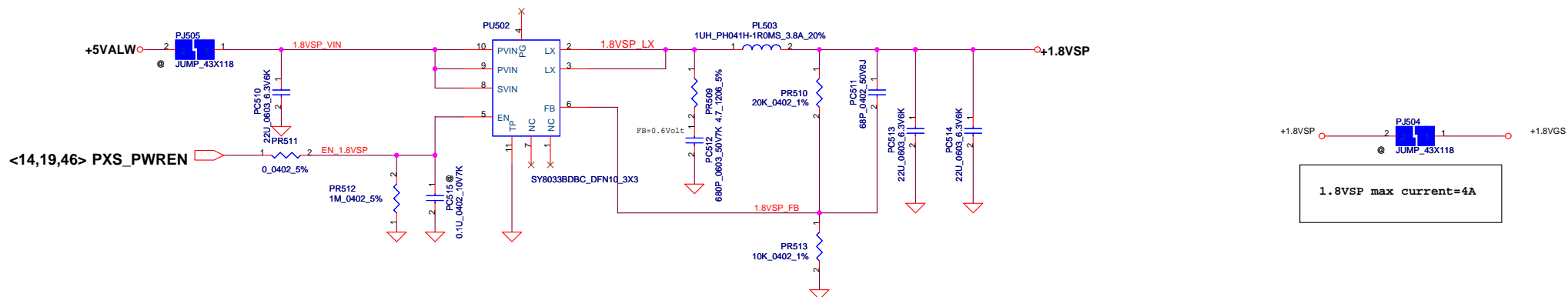
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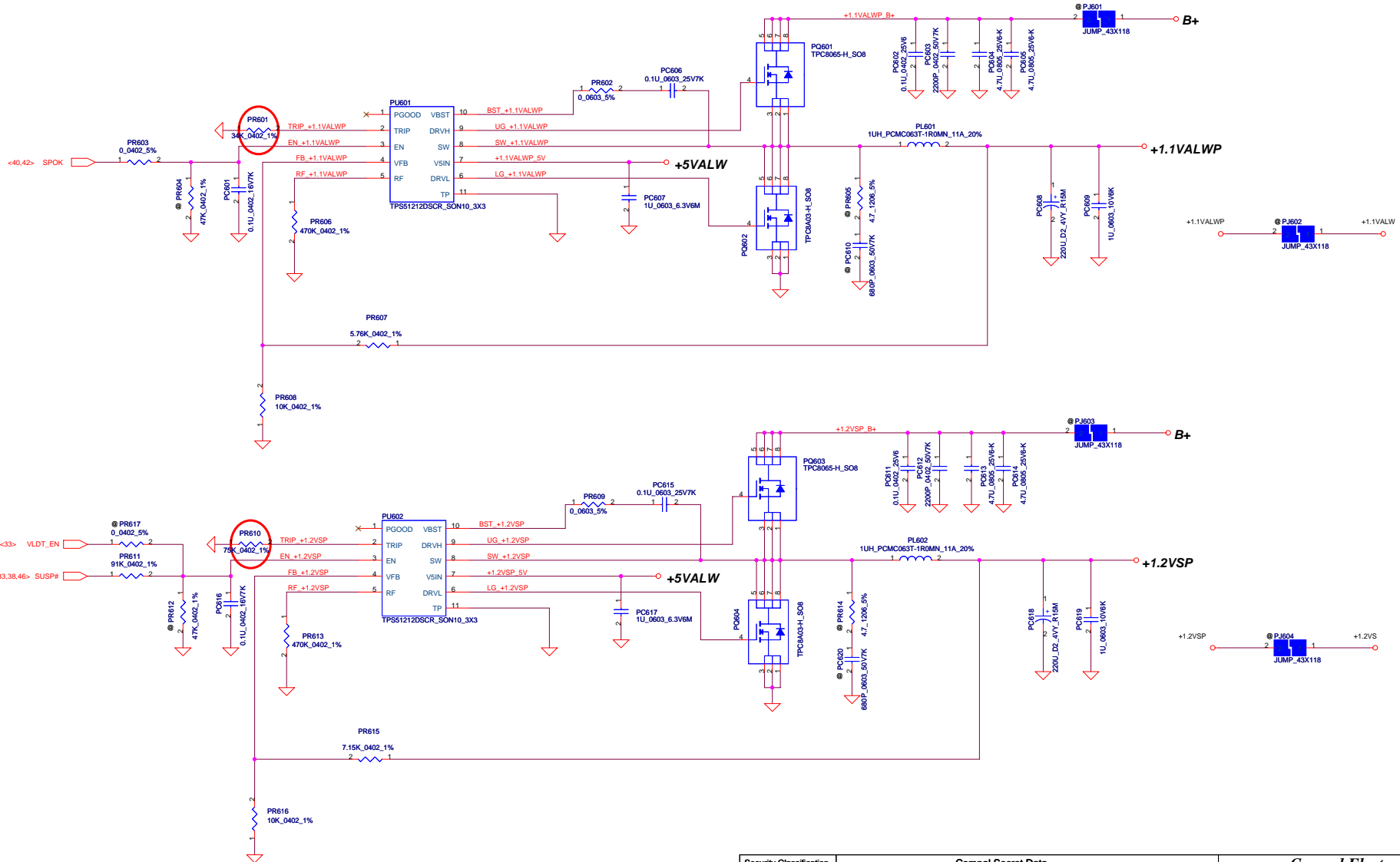


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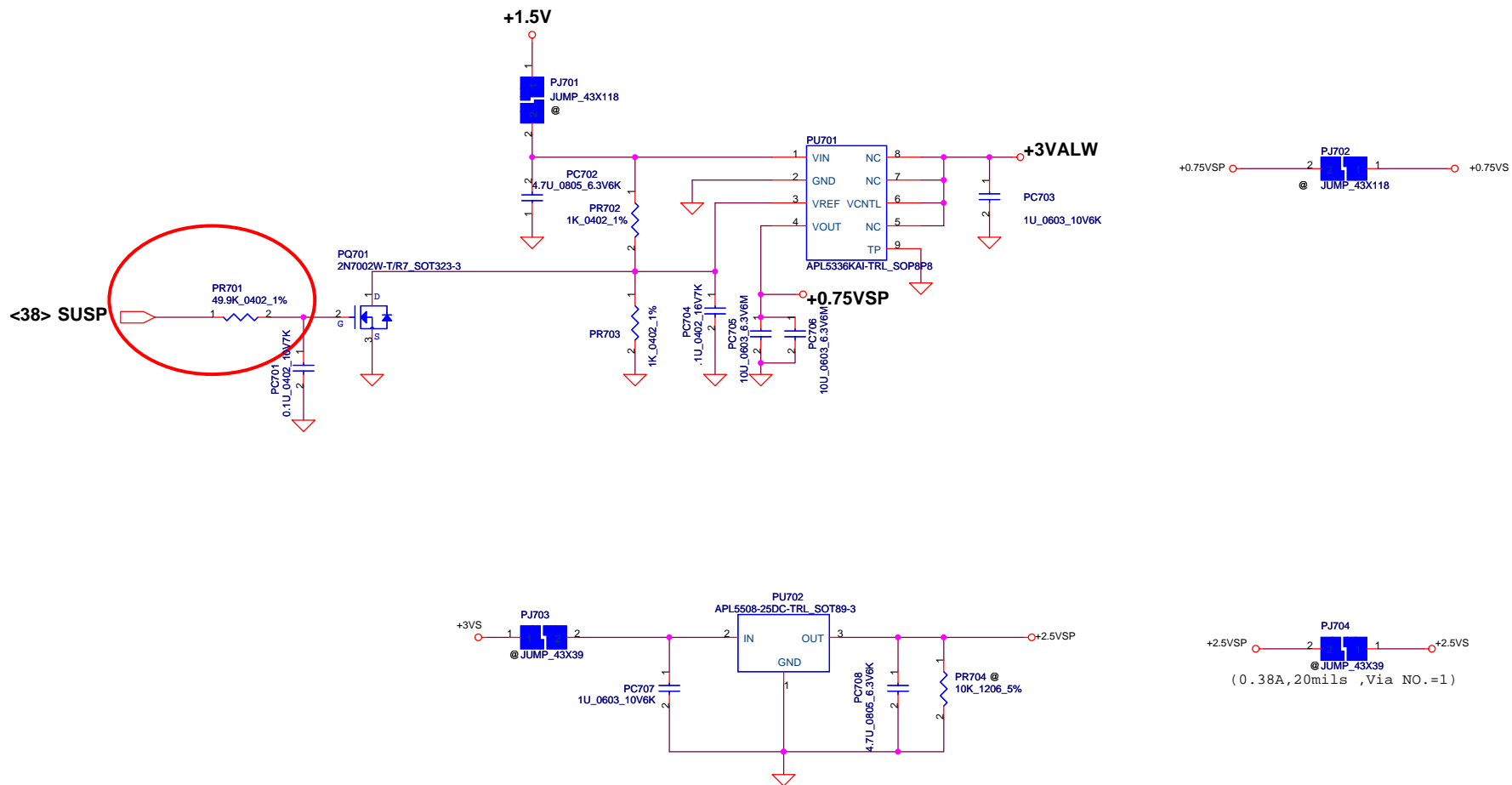


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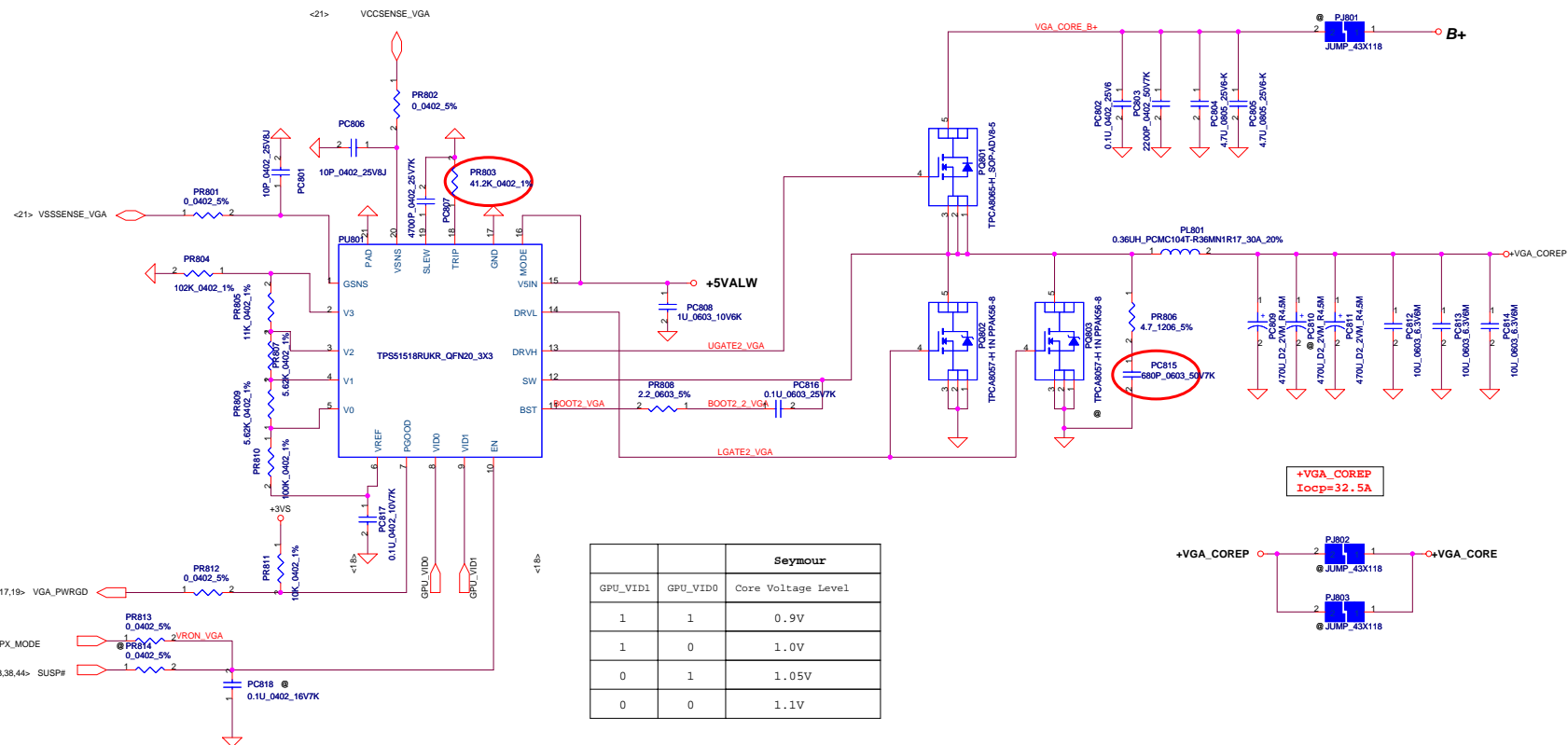


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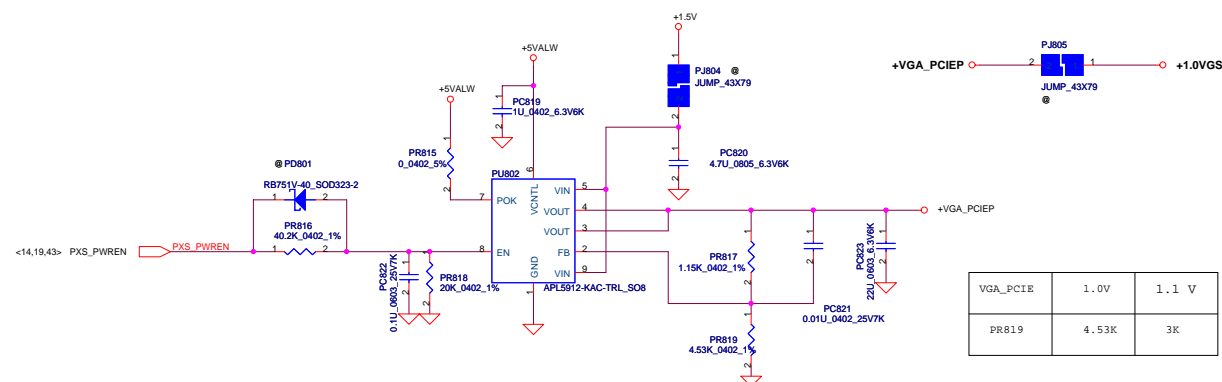




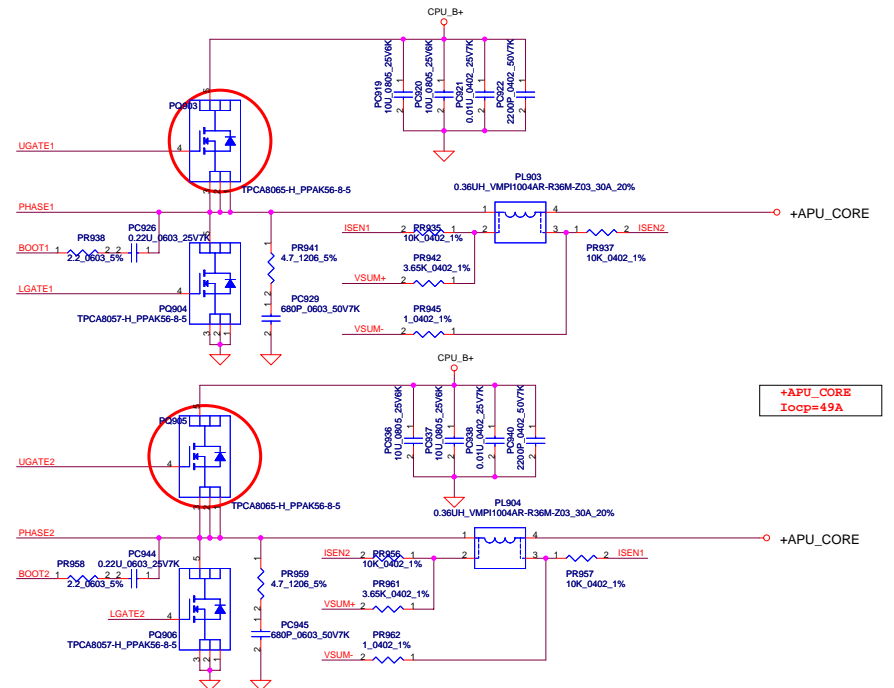
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Seymour		
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.05V
0	0	1.1V



VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K



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